SYNOPSYS®

SUCCESS STORY

Synopsys and Socionext

Ensuring Testability of an Ultra Large Scale HBM-Based Multi-Die SoC for AI and HPC

"Multiple design groups from Socionext and Synopsys collaborated as a cross-functional team to satisfy the design for test (DFT) requirements on a challenging multi-die system-on-chip (SoC) project with a master die chiplet and four High Bandwidth Memory (HBM) modules. We completed all DFT items and successfully shipped the product on schedule, at the target data rate, and without any impact on logic die size."

~Shinichiro Ikeda, Senior Principal Engineer, Socionext Inc.

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Challenges

The trends driving ultra large scale system-on-chip (SoC) designs include advanced applications such as artificial intelligence (AI) and high performance computing (HPC) with the need for multi-terabyte/second memory bandwidth. To satisfy these needs, die-to-die (D2D) chiplet technology is required to connect these SoCs with High Bandwidth Memory (HBM). To satisfy these demands, Socionext developed a 2.5D chiplet-based SoC containing a master die and four HBM modules. Such a device could not be tested in production using conventional single-die methods, so a comprehensive design for excellence (DFX) strategy was required.

Project Overview

The Socionext ultra large scale SoC is shown in Figure 1. There are 1700 High Bandwidth Interconnect (HBI) signal connections between the master die and each HBM module, for a total of 6800 within the multi-die package. None of these are accessible on production automatic test equipment (ATE), one of the reasons that an innovative DFX approach was needed. Design for test (DFT) had to support test and analysis of the HBM as well as test, analysis, and repair of the HBI. The overall package was 4.225mm2 (65mm by 65mm) in size, with a total of 4,040 solder balls in a ball grid array (BGA) configuration.

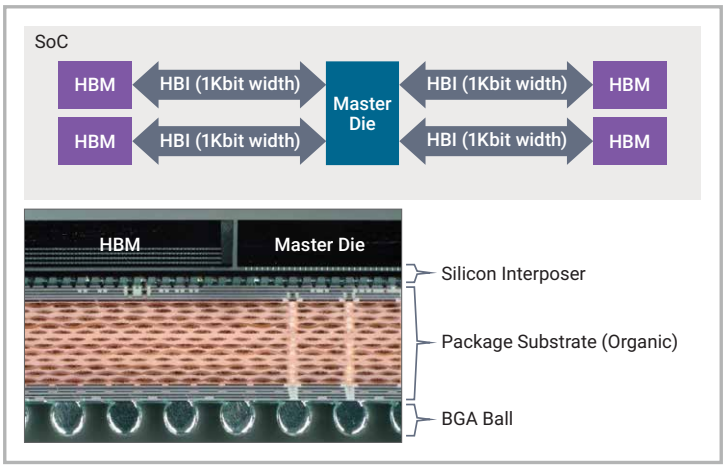

Figure 1: Overview of the Socionext multi-die design

One of the key project goals was that the overall test strategy be part of an integrated Silicon Lifecycle Management (SLM) flow to manage yield and risk. Along with the Synopsys partnership, Socionext, as the silicon provider, worked closely with both its SoC customer and the HBM DRAM vendor to meet the design, production/manufacturing test, and in-field requirements. A key benefit of a comprehensive SLM flow is that it enables the end customer to perform test and repair during the in-field stage, with failure analysis results being passed back to all parties for improvements in production test and future designs.

As shown in Figure 2, different test strategies were required for the wafer test of the master die chiplet and the final shipping test of the assembled multi-die SoC. Although the chiplet is a single die, wafer test was a challenge since the 1700 HBI bumps were too numerous and with too narrow a die pitch to be probed. Another method had to be found to test the HBM physical layer (PHY) in the master die and the interface itself. Since the memory interfaces are internal to the SoC package, they cannot be probed in final test either.

Fortunately, the HBM standard includes the ability to test and lane repair a failed HBI connection without probing, even after the master die and the HBM module are assembled into the SoC package. The standard also defines the Direct Access (DA) port in addition to the HBI signals. This port enables the HBM vendor to test and diagnose the memory cell array even after package assembly.

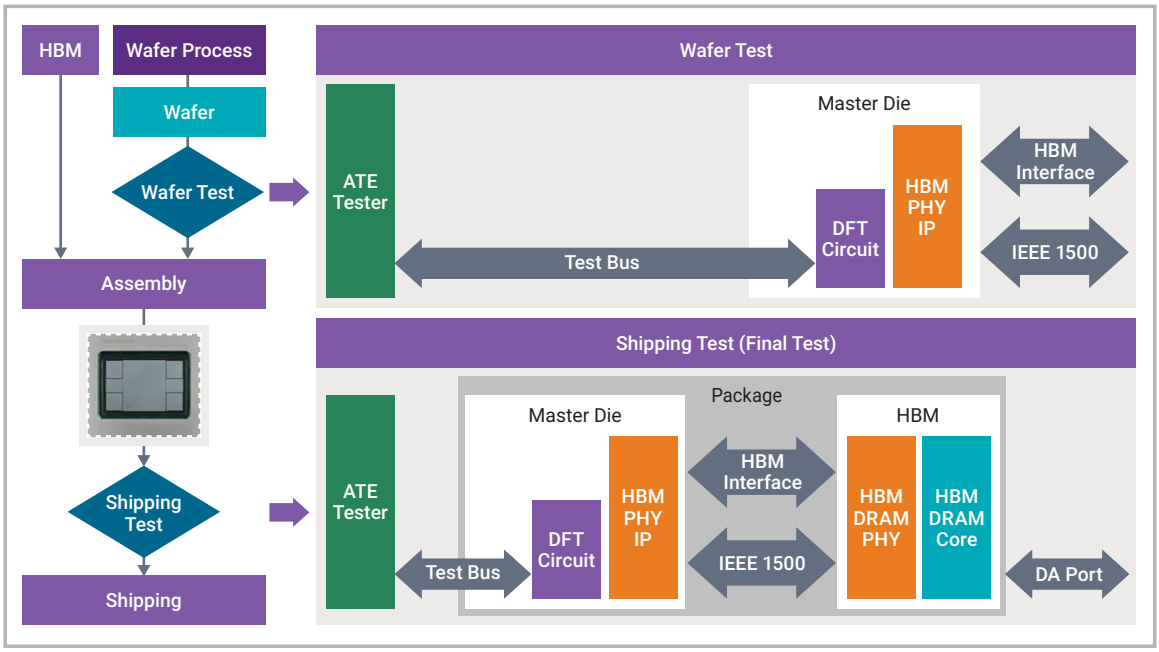

Figure 2: Test strategy for the Socionext master die and assembled SoC

The Synopsys Solution

Multiple design groups from Socionext and Synopsys formed a single cross-functional team to codify the DFX requirements and identify a solution. The experts on this team had a broad range of knowledge, including HBM DFT requirements, HBM PHY IP, electronic design automation (EDA) DFT tools, multi-die packaging, and production manufacturing. Their solution started with the selection of SLM IP from Synopsys to satisfy overall DFX requirements without any impact on memory bandwidth or die size. For the master die, the team chose the Synopsys HBM PHY IP as well as the following IP:

- Synopsys SLM SHS IP, an automated hierarchical test solution for efficiently testing SoCs with multiple analog/mixed-signal, digital logic, and interface IP by creating a hierarchical IEEE 1500 network with pre-validated production ready ATE patterns with automated pattern porting
- Synopsys SLM SMS ext-RAM IP, for high-coverage, cost-effective test, repair, and diagnostics of external (e.g., DRAM) memory and interconnect

Figure 3 shows how this IP was employed to provide DFX support for the overall test flow. Test for the digital portion of the master die was performed using conventional methods, and memory fault diagnosis used existing DA-based vendor solutions. Synopsys SHS IP was used to test the HBM PHY within the master die during wafer test without requiring wafer probe access to the HBI. Synopsys SHS IP was also used to test and perform lane repair of the HBI connections during both wafer test and final test. Test of the packaged DRAM memory arrays during final test was supported by Synopsys SMS ext-RAM IP. All IP was inserted into the register transfer level (RTL) design of the master die by leveraging the automated insertion tools provided with the Synopsys SHS IP.

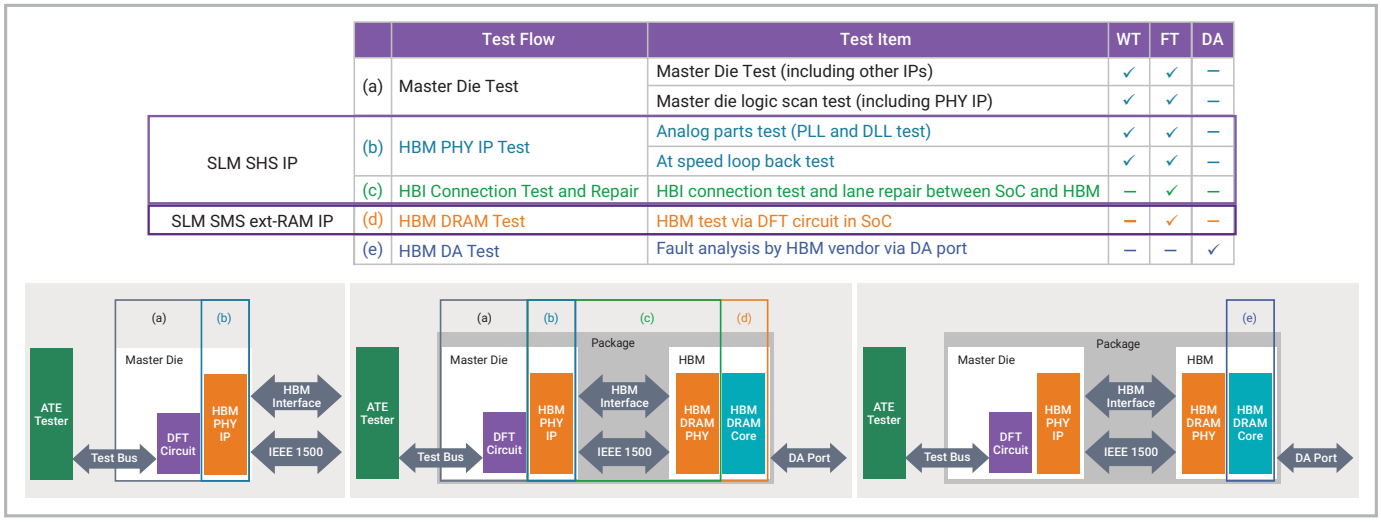

Figure 3: Types of tests supported for the Socionext master die and SoC

Expertise and Technical Support

Socionext engaged with Synopsys early in the SoC development project to learn more about the challenges of testing such an advanced device and to investigate possible solutions. For smooth project execution, the Socionext engineers required seamless support from the Synopsys IP and EDA groups. As mentioned earlier, the two companies formed a cross-functional combined team. Specific areas of collaboration included:

- In-design stage: in-field test and repair requirements, chiplet DFT strategy, and chiplet integration plan
- In-production stage: test and repair strategy, chiplet failure analysis, and HBM failure analysis
- In-field stage: SoC test and repair, chiplet failure analysis, and HBM failure analysis

The team also developed a strategy for bottom-up construction and validation of the test scenarios needed at each stage. This included combining test scenario parts and using hierarchical test pattern generation and verification for both wafer test and shipping/final test. Figure 4 provides some additional details about the overall collaborative effort among the many experts involved in the project.

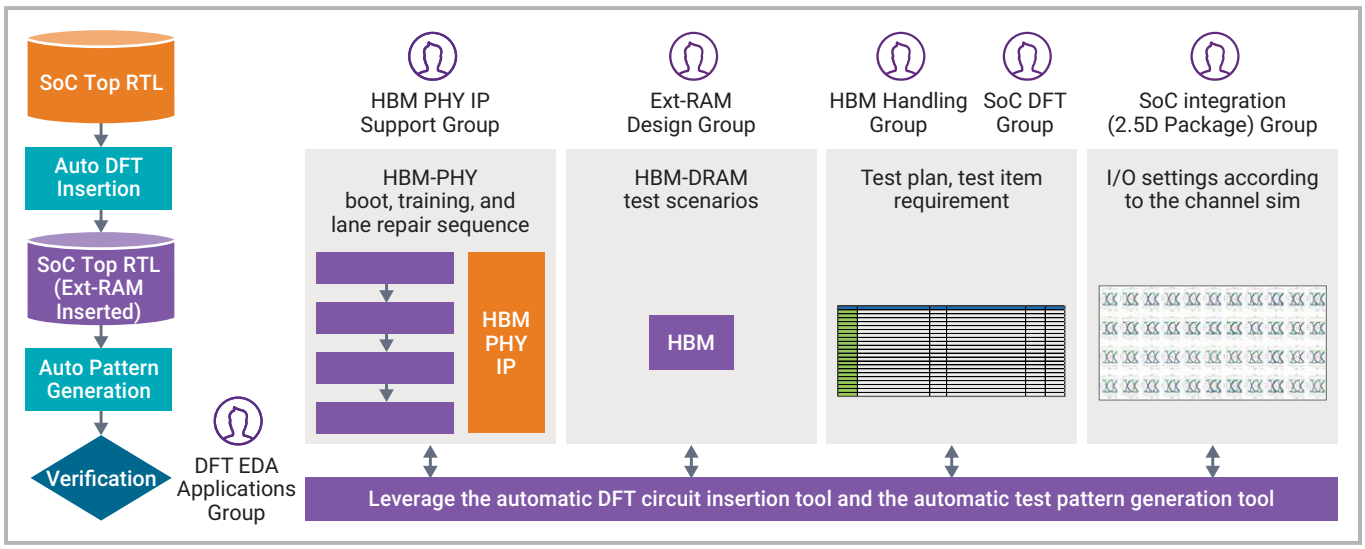

Figure 4: Cross-functional collaboration across Socionext and Synopsys groups

Summary

With the right set of Synopsys SLM IP products (SLM SHS IP and SLM SMS ext-RAM IP) and the benefits of the cross-functional team, Socionext successfully developed and shipped its first multi-die SoC with HBM on schedule. The resulting design achieved the target memory data rate of 3.6Gbits/second with no impact to the size of the master die or the packaged SoC. Socionext considers this project fully successful on all fronts and presented the results at a recent Synopsys Users Group (SNUG) event.

Socionext engineers are continuing their close collaboration with Synopsys and are currently expanding their usage of Synopsys SLM IP to even more complicated projects. Multiple logic dies, more HBM modules, and faster versions of the HBM standard are all likely future requirements. Socionext is also looking to Synopsys for Universal Chiplet Interconnect Express (UCIe) IP, advanced chiplet assembly technology, and further advances in chiplet design and DFX. There are new challenges ahead, but the collaboration between Socionext and Synopsys is now well established to replicate continued success.