ETHERNET TESTING SERVICES

Embedded MAU Test Suite
Version 5.2
Technical Document

Last Updated: September 23, 2010

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MODIFICATION RECORD

September 23, 2010

Version 5.2 Released (Beckwith)

Modifications since last release:

Added 10BASE-Te MAU to test 14.1.3, added reference to 802.3az
Added 10BASE-Te TPM to Appendix A
Updated references to 802.3-2008

August 1, 2008

Version 5.1 Released

Modifications since last release:

Reworded test 14.1.1 to reflect the correct procedure

February 9, 2006 Version 5.0 Released

Modifications since last release:

Added copyright to cover page
Updated references to 802.3-2005
Changed test 14.2.3 from "Differential Output Impedance" to "Differential Input Impedance"
Changed all references to [1], [2], etc. and updated appropriate references in text.
Made editorial changes to all tests
Added tests 14.1.12, 14.1.13

July 20, 2004 Version 4.1 Released

Modifications since last release:

Updated cover page with IOL logo
Reworded test 14.3.3 to reflect the correct procedure

January 3, 2002 Version 4.0 Released

Modifications since last release:

Updated to IEEE Std. 802.3, 2000 Edition
Removed Test 14.1.9, TD Circuit Common-Mode Output Voltage

June 30, 1999 Version 3.3 Released

Modifications since last release:

Renumbered all tests to reflect numbering scheme employed by Fast Ethernet Consortium reports.
Restructured test sequences to follow listing of test cases in 1803.3d-1993 supplement.
Added Test 14.1.1, TP_IDL Silence Duration and Silence Voltage
Added Test 14.1.9, TD Circuit Common-Mode Output Voltage
New structure:

Transmit Functions and Transmitter Specifications
- 14.1.1 TP_IDL, Silence Duration and Silence Voltage
- 14.1.2 TD Short Circuit Fault Tolerance
- 14.1.3 Peak Differential Output Voltage on the TD Circuit
- 14.1.4 Harmonic Content, All Ones (or all zeroes) Signal
- 14.1.5 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template

14.1.6 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template inverted template)
14.1.7: Transmitter Waveform for Start of TP_IDL with Specified Loads, with and without the Twisted Pair Model
14.1.8: TD Circuit Differential Output Impedance
14.1.9 TD Circuit Common-Mode Output Voltage
14.1.10 Link Test Pulse Waveform, with Specified Loads, with and without TPM
14.1.11 Transmitter Output Timing Jitter with Twisted Pair Model
14.1.12 Transmitter Output Timing Jitter without Twisted Pair Model
Receiver Functions and Receiver Specifications
14.2.1 RD Short Circuit Fault Tolerance
14.2.2 RD Circuit Signal Acceptance
14.2.3 RD Circuit Differential Input Impedance
14.2.4 RD Circuit Link Test Pulse Acceptance
Link Integrity Test Functions
14.3.1 Link Loss Timer
14.3.2 Acceptance Range for Consecutive Link Test Pulses
14.3.3 Link Test Pulses Outside Acceptance Range (not in the Link Test Pass state)
14.3.4 Value of "lc_max"
14.3.5 Link Fail Effect on Transmit Functions
14.3.6: Link Fail Effect on Receive Functions

March 26, 1998 Version 3.2 Released

Modifications since last release:

Removed Test 9.14, Signaling Rate during Transmission of Preamble

October 17, 1997 Version 3.1 Released

Modifications since last release:

Added Test 9.14, Signaling Rate during Transmission of Preamble

August 20, 1997 Version 3.0 Released

Modifications since last release:

Removed Test 8.14, Power Cycle Effect on the TD Circuit (not accurate)

Added Test 11.14, TD Circuit Differential Output Impedance
Added Test 15.14, RD Circuit Differential Input Impedance
Other tests renumbered accordingly:

Test Group 1: Transmit Functions and Transmit Specifications
1.14 TD Short Circuit Fault Tolerance
2.14 Transmitter Waveform for Start of TP_IDL with Specified Loads, with and without the Twisted Pair Model
3.14 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template
4.14 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template (inverted template)
5.14 Peak Differential Output Voltage on the TD Circuit
6.14 Transmitter Output Timing Jitter with Twisted Pair Model
7.14 Transmitter Output Timing Jitter without Twisted Pair Model
9.14 Harmonic Content, All Ones (or all zeroes) Signal
Link Test Pulse Waveform, with Specified Loads, with and without TPM
11.14 TD Circuit Differential Output Impedence
Receiver Functions and Receiver Specifications
12.14 RD Short Circuit Fault Tolerance
13.14 RD Circuit Signal Acceptance
RD Circuit Link Test Pulse Acceptance
15.15 RD Circuit Differential Input Impedance
Link Integrity Test Functions
16.14 Link Loss Timer
17.14 Acceptance Range for Consecutive Link Test Pulses
18.14 Link Test Pulses Outside Acceptance Range (not in the Link Test Pass state)
19.14 Value of "lc_max"
20.14 Link Fail Effect on the Transmit Functions
21.14 Link Fail Effect on the Receive Functions

September 6, 1996 Version 2.0 Released

Modifications since last release:

Added Test 19.14, Link Fail Effect on the Receive Functions

August 9, 1996 Version 1.1 Released

Modifications since last revision:

Test 13.14 added more link test pulse shapes not previously defined

February 9, 1996 Version 1.0 Released

Initial Release

Test Group 1: Transmit Functions and Transmit Specifications
- 1.14 TD Short Circuit Fault Tolerance
- 2.14 Transmitter Waveform for Start of TP_IDL with Specified Loads, with and without the Twisted Pair Model
- 3.14 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template
- 4.14 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template (inverted template)
- 5.14 Peak Differential Output Voltage on the TD Circuit
- 6.14 Transmitter Output Timing Jitter with Twisted Pair Model
- 7.14 Transmitter Output Timing Jitter without Twisted Pair Model
- 8.14 Power Cycle Effect on the TD Circuit
- 9.14 Harmonic Content, All Ones (or all zeroes) Signal
- 10.14 Link Test Pulse Waveform, with Specified Loads, with and without TPM

Receiver Functions and Receiver Specifications
- 11.14 RD Short Circuit Fault Tolerance
- RD Circuit Signal Acceptance
- 13.14 RD Circuit Link Test Pulse Acceptance

Link Integrity Test Functions
- 14.14 Link Loss Timer
- 15.14 Acceptance Range for Consecutive Link Test Pulses
- 16.14 Link Test Pulses Outside Acceptance Range (not in the Link Test Pass state)
- Value of “lc_max”
- 18.14 Link Fail Effect on the Transmit Functions

ACKNOWLEDGMENTS

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Jon Beckwith	University of New Hampshire
Nate Bourgoine	University of New Hampshire
Adam Healey	University of New Hampshire
Bob Noseworthy	University of New Hampshire
Gary Pressler	University of New Hampshire
Neal Starr	University of New Hampshire

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functioning of their Clause 14 Medium Attachment Unit, Type 10BASE-T based products. The tests do not determine if a product conforms to the IEEE 802.3 standard, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within 10BASE-T physical layer device. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other Clause 14 10BASE-T MAUs. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most 10BASE-T environments. The IEEE 802.3az Energy Efficient Ethernet Standard has added a type 10BASE-Te MAU, which has the same requirements as 10BASE-T but uses a lower output amplitude (see test #14.1.3).

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross-references to the IEEE 802.3 standards and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification

This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists observables that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems
This section contains a description of known issues with the test procedure, which may effect test results in certain situations.

TABLE OF CONTENTS

GROUP 1: TRANSMIT FUNCTIONS AND TRANSMIT SPECIFICATIONS

Scope: The following tests cover 10BASE-T operation specific to transmission characteristics on the TD circuit.

Overview: These tests are designed to verify that the device under test transmits various defined waveforms properly and to verify transmitted signal parameters.

Test #14.1.1: TP_IDL, Silence Duration and Silence Voltage

Purpose: To verify the timing of signals following the start of TP_IDL.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.1, Test Case ID 1411.01.06
[2] IEEE Std 802.3™-2008: Section 14.2.1.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

Once a device has sourced a start of TP_IDL signal from the TD circuit, it should be followed by a 16 ms ±8 ms period of silence and a link test pulse.

Test Setup:

Setup the devices as shown in Fig. 14.1.1-1. The TP test card is used for LTP generation and line termination for the DUT's TD circuit. The TD circuit should be terminated with either of the test loads defined in Figure 14-11 in reference [2]. Observations of the TD circuit are made with a differential probe across the circuit termination. The TP test card additionally contains a Twisted Pair Model which may be added to the TD circuit before termination.

In cases where frame sourcing cannot be accomplished through the device itself, a cable which splits the transmit and receive pairs of the device to two different cables is used. This allows for a traffic generator to send frames to the device and the device's response to be seen on the TP card. The LTP generation of the TP card is then used to provide a link to the traffic generator. This setup is shown in figure 14.1.1-1 (b).

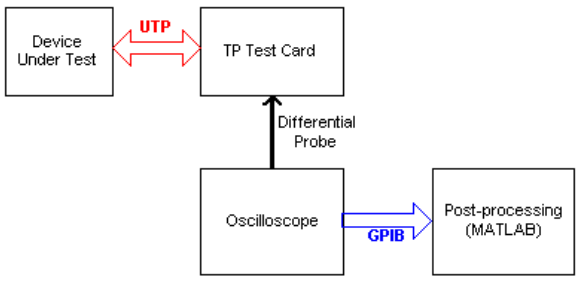

Figure 14.1.1-1 (a): Test Setup A

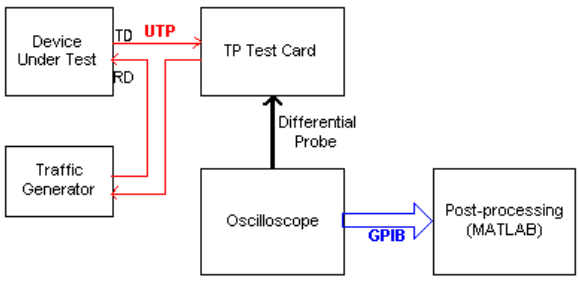

Figure 14.1.1-1 (b): Test Setup A (alternate setup)

Procedure:

1. While sourcing data from the TD circuit, terminate it with a 100 Ω resistive load.
2. Measure the period of time from the start of TP_IDL to the next transmitted link test pulse.
3. Measure the period of time between repeating link test pulses.
4. Measure the differential voltage during TD circuit silence between link test pulses.

Observable Results:

- The measured time period between start of TP_IDL and first link test pulse shall be 16 ms ±8 ms.
- All repeating link test pulses shall be transmitted every 16 ms ±8 ms.
- The differential voltage of the TD circuit shall remain at 0 mV ±50 mV during the periods of silence between consecutive link test pulses.
- The differential voltage of the TD circuit shall remain at 0 mV ±50 mV during the periods of silence between an SOI and the following LTP.

Test #14.1.2: TD Short Circuit Fault Tolerance

Purpose: To verify transmitter tolerance to short circuits.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.01
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.7

Resource Requirements:

- Current probe
- Oscilloscope

Last Modification: January 26, 2006

Discussion:

Transmitters shall be able to withstand short circuits for indefinite periods of time without suffering damage. After such a fault is removed, normal operation of the transmitter shall resume.

Test Setup:

Setup the devices as shown in Fig. 14.1.2-1. The TP test card is used for LTP generation.

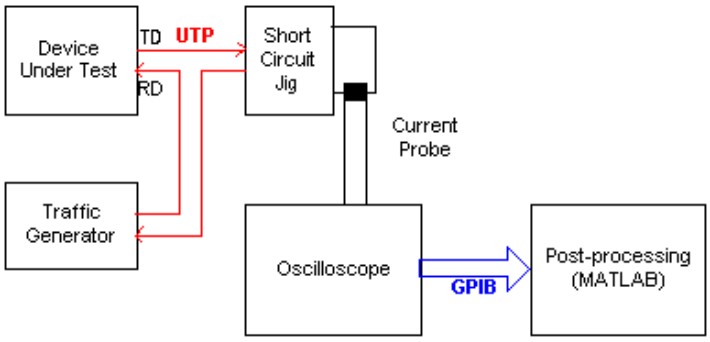

Figure 14.1.2-1: Test Setup B

Procedure:

1. Supply power to the device under test.
2. Apply a short circuit across the TD circuit for 10 seconds.
3. Monitor the peak output current of the TD circuit.
4. Continue to monitor the output current for an additional 10 seconds while trying to source data from the TD circuit.
5. Remove the short circuit.
6. Verify that the transmitter operates normally by performing other transmitter tests.

Observable Results:

- The magnitude of the current going through the short circuit shall not exceed 300 mA.
- The station under test shall function properly during other transmitter tests.

Test #14.1.3: Peak Differential Output Voltage on the TD Circuit

Purpose: To verify the peak differential output voltage on the TD circuit.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.02
[2] IEEE Std 802.3™-2008 Section 14.3.1.2.1
[3] IEEE Std P802.3AZ-D3.2, Clause 14

Resource Requirements:

- Oscilloscope
- Differential Voltage Probes
- TP Test Card

Last Modification: August 4, 2010

Discussion:

For a 10BASE-T MAU, the peak differential voltage output on a TD circuit shall be between 2.2 V and 2.8 V for all data sequences when terminated with a 100 Ω resistive load. For a 10BASE-Te MAU, the peak differential voltage output on a TD circuit shall be between 1.54 V and 1.96 V for all data sequences when terminated with a 100 Ω resistive load

Test Setup: See Figure 14.1.1-1.

Procedure:

1. While sourcing data from the TD circuit, terminate it with a 100 Ω resistive load.
2. Measure the peak differential output voltage across the TD circuit.

Observable Results:

- For a 10BASE-T MAU, the magnitude of the measured peak positive and negative differential voltage across the TD circuit shall fall between 2.2 V and 2.8 V.
- For a 10BASE-Te MAU, the magnitude of the measured peak positive and negative differential voltage across the TD circuit shall fall between 1.54 V and 1.96 V.

Test #14.1.4: Harmonic Content, All Ones (or All Zeroes) Signal

Purpose: To verify the harmonic content of the output signal.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.03
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

When monitoring a series of all ones (or all zeroes) on the TD circuit, each harmonic shall be at least 27 dB below the 10 MHz fundamental.

Test Setup: See Figure 14.1.1-1.

Procedure:

1. Source data from the TD circuit.
2. Find a portion of the packet which contains 20 cycles of all ones (or all zeroes).
3. Compute the power contained within the fundamental frequency component of the all-zeros portion.
4. Compute the power contained within the other harmonics within the frequency spectrum of the all-zeros portion.

Observable Results:

- All of the harmonics shall be at least 27 dB below the fundamental.

Test #14.1.5: Differential Output Waveform on the TD Circuit with Scaling of Voltage Template.

Purpose: To verify that the transmitter output equalization meets standard specifications.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.04
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

The eye pattern sourced from the TD circuit shall conform to defined templates in Figure 14-9 of reference [2].

Test Setup: See Figure 14.1.1-1.

Procedure:

1. While sourcing data from the TD, terminate it with a 100 Ω resistive load and with the TPM.
2. Accumulate an eye pattern on the oscilloscope with the triggering set to zero volts and a positive slope.

Observable Results:

- The voltage pattern sourced from the TD circuit shall fit into the template shown in Figure 14-9 of reference [2].

Test #14.1.6: Differential Output Waveform on the TD Circuit with Scaling of Voltage Template (inverted template)

Purpose: To verify that the transmitter output equalization meets standard specifications.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.05
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

The eye pattern sourced from the TD circuit shall conform to defined inverted templates in Figure 14-9 of reference [2].

Test Setup: See Figure 14.1.1-1.

Procedure:

1. While sourcing data from the TD circuit, terminate it with the TPM and a 100 Ω resistive load.
2. Accumulate an eye pattern on the oscilloscope with the triggering set to zero volts and a negative slope.

Observable Results:

- The voltage pattern sourced from the TD circuit shall fit into the template shown in Figure 14-9 of reference [2].

Test #14.1.7: Transmitter Waveform for Start of TP_IDL with specified loads, with and without the Twisted Pair Model

Purpose: To verify that the transmitter functions properly after a transition to the idle state**.**

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.06
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

After the transmission of a packet, a TP_IDL signal is transmitted. This start of TP_IDL signal shall fit into a defined template. Prior to the start of TP_IDL, two scenarios are observed: one where the entry to the template is after a wide pulse shape and one where the entry is after a narrow pulse shape. Here, these two cases are observed independently.

Test Setup: See Figure 14.1.1-1.

Procedure:

1. Monitor the TD circuit while data packets are being transmitted.
2. Observe the TP_IDL waveform following a wide pulse at the end of the packets.
3. For enhanced accuracy, multiple averages may be taken.
4. Repeat the procedure using a narrow pulse preceding the start of TP_IDL.
5. Repeat steps 1-4 using each test load defined in Figure 14-10 of reference [2].
6. Repeat steps 1-5 with the loads connected through the TPM.

Observable Results:

- The observed TP_IDL pattern shall fit into the template defined in Figure 14-10 of reference [2] for both entry shapes, across all test loads, with the TPM.
- The observed TP_IDL pattern shall fit into the template defined in Figure 14-10 of reference [2] for both entry shapes, across all test loads, without the TPM.
- After the voltage has gone below -50 mV, it shall remain below +50 mV during the TP_IDL waveform.

Test #14.1.8: TD Circuit Differential Output Impedance

Purpose: To verify the transmitter differential output impedance**.**

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.07
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.2

Resource Requirements:

- Network Analyzer
- Balun
- 100Base-Tx PMD Test Jig (refer to PMD Test Suite)

Last Modification: January 26, 2006

Discussion:

Whenever the MAU is powered, the differential output impedance, as measured on the TD circuit, must meet the following specifications: Any reflection on the TD circuit of a simplex link segment having any impedance between 85 Ω and 111 Ω must be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz.

Test Setup:

Setup the devices as shown in Figure 14.1.8-1. The balun is used to convert the 50 Ω unbalanced output from the network analyzer to the 100 Ω balanced UTP cable.

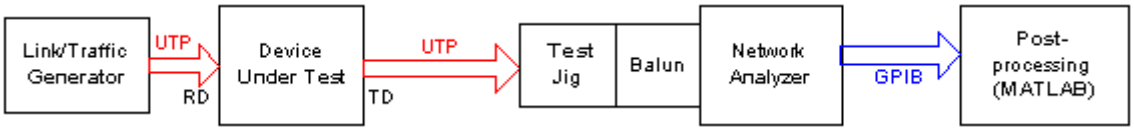

Figure 14.1.8-1: Test Setup C

Procedure:

1. Calibrate the network analyzer with the balun and twisted pair cable between the analyzer and the calibration loads.
2. Connect the TD circuit of the DUT to the twisted pair cable and terminate the RD circuit with a 100 Ω resistive load. Be sure the DUT is powered on.
3. Set the network analyzer to measure reflections from 5.0 MHz to 10 MHz at its reference resistance.
4. Use the analyzer data to calculate the return loss for source impedances of 100 Ω, 85 Ω, and 111 Ω.
5. Repeat using a frame containing all ones as the data portion, then using 01.

Observable Results:

- The return loss for the TD circuit must be at least 15 dB below the incident while idle and transmitting over the range of 5.0 MHz to 10 MHz for each of the reference resistances: 100 Ω, 85 Ω, and 111 Ω.

Test #14.1.9: Link Test Pulse Waveform, with Specified Loads, with and without TPM

Purpose: To verify that the link test pulse waveforms meet specification.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.11
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.1

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

There are waveform specifications in reference [2] to which all link test pulses need to conform. This test is designed to verify that the station under test produces link test pulses within specification.

Test Setup: See Figure 14.1.1-1.

Procedure:

1. Monitor the TD circuit while no data is being transmitted.
2. Observe the link test pulse waveforms on the TD circuit across each test load defined in Figure 14-11 of reference [2].
3. Repeat procedure with the loads connected through the TPM.

Observable Results:

- Under each test setup, the link test pulse waveforms shall fit within the template defined in Figure 14-12 of reference [2].
- After the differential output voltage drops below -50 mV, it shall remain below +50 mV.

Test #14.1.10: Transmitter Output Timing Jitter with Twisted Pair Model

Purpose: To verify that the timing of zero crossings on the TD circuit occurs within specification.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.12
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.3, B.4.1, B.4.3.3

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

All zero crossings of the TD signal shall occur with timing specification. This is verified by measuring the zero crossings at 8.0 and 8.5 bit times (BT) and making sure these times fit within specification. This test does not apply to the first bit transmitted, so this bit is disregarded.

Test Setup: See Figure 14.1.1-1.

Procedure:

1. While sourcing data from the TD circuit, terminate it with a 100 Ω resistive load and with the TPM.
2. Set the oscilloscope to trigger at zero voltage and a positive slope.
3. While sourcing data, use the oscilloscope to measure the output timing jitter of the TD circuit.
4. Observe the zero crossings at 8.0 and 8.5 BT after the triggering zero crossing.

Observable Results:

- Zero crossings shall occur at 8.0 BT ±11 ns and 8.5 BT ±11 ns after the triggering zero crossing.

Test #14.1.11: Transmitter Output Timing Jitter without Twisted Pair Model

Purpose: To verify that the timing of zero crossings on the TD circuit occurs within specification.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.13
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.3, B.4.1, B.4.3.3

Resource Requirements:

- Oscilloscope
- Differential Voltage Probe
- TP Test Card

Last Modification: January 26, 2006

Discussion:

All zero crossings of the TD signal shall conform to timing standards. This is verified by measuring the zero crossings at 8.0 and 8.5 bit times (BT) and making sure these times fit within specification. This test does not apply to the first bit transmitted, so this bit is disregarded.

Test Setup: See Figure 14.1.1-1.

Procedure:

1. While sourcing data from the TD circuit, terminate it with a 100 Ω resistive load but without the TPM.
2. Set the oscilloscope to trigger at zero voltage and a positive slope.
3. While sourcing data, use the oscilloscope to measure the output timing jitter of the TD circuit.
4. Observe the zero crossings at 8.0 and 8.5 BT after the triggering zero crossing.

Observable Results:

- Zero crossings shall occur at 8.0 BT ±20 ns and 8.5 BT ±20 ns after the triggering zero crossing.

Test #14.1.12: Transmitter Impedance Balance

Purpose: To verify that the common-mode to differential-mode impedance balance of the TD circuit is greater than the specified limit.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.08
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.4

Resource Requirements:

- Network Analyzer
- Balun
- Test Jig

Last Modification: January 26, 2006

Discussion:

The common-mode to differential-mode impedance balance of the TD circuit shall exceed the limit shown below over the frequency range of 1.0 MHz to 20 MHz. The balance is defined as $20\log_{10}(E_{cm}/E_{dif})$, which is measured by performing an S21 measurement on a Vector Network Analyzer.

Test Setup:

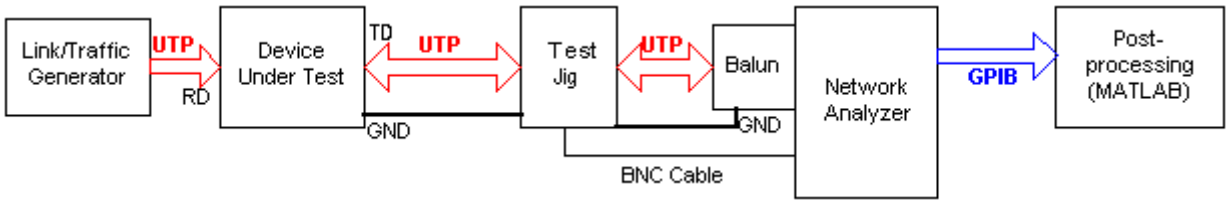

Figure 14.1.12-1: Test Setup D

Procedure:

1. Configure the device for 10Base-T operation.
2. Setup the device as shown in figure 14.1.12-1.
3. Measure E_{dif} over the specified frequency range.
4. Compute the Impedance Balance.
5. Repeat while the device is actively transmitting.

Observable Results:

- The common-mode to differential-mode impedance balance of the TD circuit shall exceed $20-17\log_{10}(f/10)$ (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 20 MHz.

Test #14.1.13: Common-mode Output Voltage

Purpose: To verify that the common-mode output voltage is less than the specified limit.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.10, Test Case ID 1411.10.09
[2] IEEE Std 802.3™-2008: Section 14.3.1.2.5

Resource Requirements:

- Oscilloscope
- BNC Cable
- Common-mode test jig

Last Modification: January 26, 2006

Discussion:

The peak common-mode voltage, measured using the setup shown in Figure 14-14 of reference [2], shall be less than 50 mV.

Test Setup:

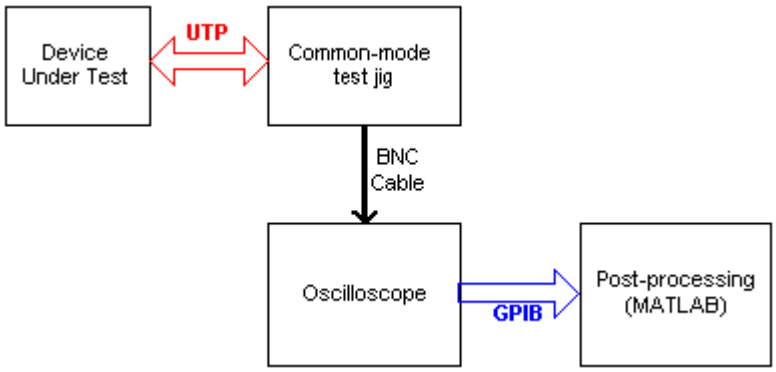

Figure 14.1.13-1: Test Setup E

Procedure:

1. Configure the device for 10Base-T operation.
2. Setup the device under test and the oscilloscope as shown in Figure 14.1.13-1.
3. Measure the common-mode output voltage on pair A.
4. For enhanced accuracy, repeat step 4 and average the results.
5. Repeat while the device is actively transmitting.

Observable Results:

- The peak common-mode output voltage shall be less than 50 mV.

GROUP 2: RECEIVER FUNCTIONS AND RECEIVER SPECIFICATIONS

Scope: The following tests cover 10BASE-T operation specific to reception functionality of the DUT.

Overview: These tests are designed to ensure correct input signal handling of the receiver.

Test #14.2.1: RD Circuit Short Circuit Fault Tolerance

Purpose: To verify receiver tolerance to short circuits.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.11, Test Case ID 1411.11.01
[2] IEEE Std 802.3™-2008: Section 14.3.1.3.6

Resource Requirements:

None

Last Modification: February 9, 1996

Discussion: The RD circuit shall be able to withstand short circuits.

Test Setup:

All that is needed is to plug a simple RJ-45 plug with a short across the RD pair into the port of the DUT.

Procedure:

1. Apply a short circuit across the RD circuit for 10 seconds.
2. Verify that the station under test still works by performing the other receiver tests.

Observable Results:

- The station under test shall perform normally for the remainder of the testing.

Test #14.2.2: RD Circuit Signal Acceptance

Purpose: To verify the receiver's differential input voltage acceptance range.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.11, Test Case ID 1411.11.03
[2] IEEE Std 802.3™-2008: Section 14.3.1.3.1

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: January 26, 2006

Discussion:

Reference [2] requires that a station accept packets with a maximum jitter allowance of 13.5 ns. This means that wide pulses may have 73 ns to 127 ns between zero crossings and narrow pulses may have 23 ns to 77 ns. This is to account for a maximum jitter allowance of ±13.5 ns. Also, these packets may have a differential voltage between 585 mV and 3.1 V.

Test Setup:

Setup the devices as shown in Fig. 14.2.2-1. The arbitrary waveform generator produces the test signals for the RD circuit. The balun is used to convert the 50 Ω unbalanced AWG output to a 100 Ω balanced UTP output onto the RD circuit. Observations of the TD circuit are made with differential probes across the 100 Ω termination on the TP test card.

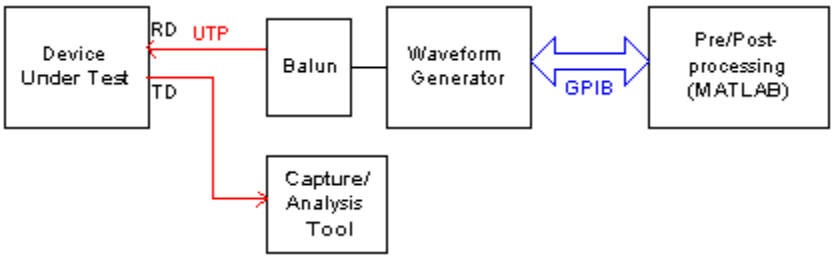

Figure 14.2.2-1: Test Setup E

Procedure:

1. This test is not currently performed.

Observable Results:

- If the DUT is set to reply to the packet sent, a reply shall be observed on the TD circuit for both voltage levels.
- If MAC layer statistics can be observed, the reception of a good packet shall be logged for both voltage levels.

Test #14.2.3: RD Circuit Differential Input Impedance

Purpose: To verify the receiver differential input impedance**.**

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.11, Test Case ID 1411.11.05
[2] IEEE Std 802.3™-2008: Section 14.3.1.3.4

Resource Requirements:

- Network Analyzer
- Balun

Last Modification: January 26, 2006

Discussion:

Whenever the MAU is powered, the differential input impedance, as measured on the RD circuit, must meet the following specifications. Any reflection on the RD circuit of a simplex link segment having any impedance between 85 Ω and 111 Ω must be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz.

Test Setup:

Setup the devices as shown in Figure 14.2.4-1. The balun is used to convert the 50 Ω unbalanced output from the network analyzer to the 100 Ω balanced UTP cable.

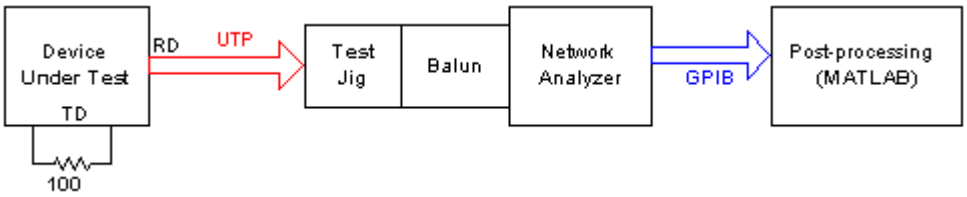

Figure 14.2.4-1: Test Setup F

Procedure:

1. Calibrate the network analyzer with the balun and twisted pair cable between the analyzer and the calibration loads.
2. Connect the RD circuit of the DUT to the twisted pair cable and terminate the TD circuit with a 100 Ω resistive load. Be sure the DUT is powered on.
3. Set the network analyzer to calculate return loss from 5.0 MHz to 10 MHz at its reference resistance.
4. Use the analyzer data to calculate the return loss for reference resistances of 100 Ω, 85 Ω, and 111 Ω.

Observable Results:

- The return loss for the RD circuit must be at least 15 dB below the incident from the range of 5.0 MHz to 10 MHz for each of the reference resistances: 100 Ω, 85 Ω, and 111 Ω.

Test #14.2.4: RD Circuit Link Test Pulse Acceptance

Purpose: To verify that the RD circuit accurately accepts link test pulses.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.11, Test Case ID 1411.10.07
[2] IEEE Std 802.3™-2008: Section 14.3.1.3.2

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: January 26, 2006

Discussion:

Link test pulses have specified characteristics to be recognized by the RD circuits. This test verifies that the station under test shall accept worst-case link test pulses. Worst-case link test pulses have one of the following sets of characteristics, as in Figure 14-14 of reference [2]:

1. Peak amplitude of 585 mV, a pulse width of 0.60 BT, and maximum undershoot.
2. Maximum allowed amplitude of 3.1V, a pulse width of 2.0 BT, and no undershoot.
3. Maximum allowed amplitude of 3.1V, a pulse width of 0.6 BT, and maximum undershoot.
4. Peak amplitude of 585 mV, a pulse width of 2.0 BT, and no undershoot.
5. Peak amplitude of 585 mV, a pulse width of 0.6 BT, and no undershoot.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Send a valid packet and monitor the TD circuit.
3. Send at least 11 of the worst case link test pulses to the RD circuit followed by a valid packet and monitor the TD circuit again.
4. Repeat Step 3 using the other worst case link test pulses.

Observable Results:

- After the packet without preceding link test pulses, there shall be no activity on the TD circuit and MAC statistics of the DUT, if available, shall display no packets received.
- The DUT shall accept and, if applicable, reply to the valid packet preceded by each case of 11 worst-case link test pulses.

GROUP 3: LINK INTEGRITY TEST FUNCTIONS

Scope: The following tests cover 10BASE-T operation specific to the functional characteristics of the Link Test functions.

Overview: These tests are designed to verify that the device under test either properly establishes and/or maintains link, or properly remains unlinked based on the test case.

Test #14.3.1: Link Loss Timer

Purpose: To verify that the value of the "link_loss" timer is within the prescribed range.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.7, Test Case ID 1411.07.01
[2] IEEE Std 802.3™-2008: Section 14.2.1.7

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: February 9, 1996

Discussion:

There is a finite time period after link test pulses end that the station under test enters the Link Test Fail state. This time is called "link_loss." The IEEE 802.3 standard allows the value of "link_loss" to be between 50 ms and 150 ms. This test is designed to determine the value of "link_loss" for the DUT and verify that it is within the specified range.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Use the AWG to generate a series of 11 link test pulses, a delay, and a valid packet.
2. Apply this signal continuously to the RD circuit of the station under test.
3. Monitor the TD circuit of the station under test and/or observe MAC statistics.
4. Vary the delay until reaching the largest value that allows all packets sent to be accepted.
5. Record this delay as the value for "link_loss."

Observable Results:

- The "link_loss" time shall be between 50 ms and 150 ms.

Test #14.3.2: Acceptance Range of Link Test Pulses

Purpose: To verify the acceptance range of link test pulses.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.7, Test Case ID 1411.07.02
[2] IEEE Std 802.3™-2008: Section 14.2.1.7

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: February 9, 1996

Discussion:

As well as characteristic requirements, link test pulses have requirements for the delay between consecutive pulses. In order to be accepted as valid, received link test pulses shall have a delay between them between "link_test_max" and "link_test_min." The value for "link_test_min" shall be between 2 ms and 7 ms. The value for "link_test_max" shall be between 25 ms and 150 ms. This test is to verify that the station under test accepts link test pulses with spacing within these ranges.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Verify that the station under test is in the Link Test Fail state.
3. Use the AWG to send at least 11 consecutive link test pulses spaced 7.1 ms apart.
4. Verify that the station under test exits the Link Test Fail state.
5. Repeat procedure using link test pulses spaced 24 ms apart.

Observable Results:

- The station under test shall exit the Link Test Fail state after receiving either set of link test pulses.

Test #14.3.3: Link Test Pulses Outside Acceptance Range (not in Link Test Pass state)

Purpose: To verify the refusal of link test pulses outside the allowed timing range.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.7, Test Case ID 1411.07.04
[2] IEEE Std 802.3™-2008: Section 14.2.1.7

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: February 9, 1996

Discussion:

As well as characteristic requirements, link test pulses have requirements for the delay between consecutive pulses. In order to be accepted as valid, received link test pulses shall have a delay between them between "link_test_max" and "link_test_min." The value for "link_test_min" shall be between 2 ms and 7 ms. The value for "link_test_max" shall be between 25 ms and 150 ms. This test verifies that the station under test will not accept link test pulses with spacing outside these ranges.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Verify that the station under test is in the Link Test Fail state.
3. Use the AWG to send at least 11 consecutive link test pulses spaced 1.9 ms apart.
4. Verify that the station under test remains in the Link Test Fail state.
5. Repeat procedure using link test pulses spaced 151 ms apart.

Observable Results:

- The station shall not exit the Link Test Fail state.

Test #14.3.4: Value of "lc_max"

Purpose: To find the value of "lc_max."

References:

[1] IEEE Std 802.3™-2008: Section 14.2.1.7

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: February 9, 1996

Discussion:

After entering the Link Test Fail State, the station under test shall receive either RD_input or some number of valid link test pulses to return to the Link Test Pass state. The number of link test pulses required is "lc_max" and may be between 2 and 10, inclusively. This test is designed to find the value of "lc_max" for the DUT.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Verify the Link Test Fail state by noticing TP_IDL on the TD circuit.
3. Use the AWG to make a series of 10 valid link test pulses with 16 ms spacing.
4. Send this sequence and verify that the station under test exits the Link Test Fail state.
5. Decrease the number of pulses in the sequence and repeat the procedure.
6. Record the lowest number of pulses that allows the station to exit the Link Test Fail state.

Observable Results:

- The number of pulses needed to exit the Link Test Fail state shall be between 2 and 10 inclusively.

Test #14.3.5: Link Fail Effect on Transmit Functions

Purpose: To verify that, while in the Link Test Fail state, transmit functions are disabled.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.7, Test Case ID 1411.07.05
[2] IEEE Std 802.3™-2008: Section 14.2.1.7

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: February 9, 1996

Discussion:

For a signal to be accepted there needs to be a link present between the two stations. A link is recognized by the reception of link test pulses or data on a station's RD circuit, else the station enters the Link Test Fail state. When in this state, transmissions to the TD circuit shall be disabled.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Verify the Link Test Fail state by noticing TP_IDL on the TD circuit.
3. Attempt to send data from the DUT.
4. Observe the TD circuit.

Observable Results:

- The TD circuit shall transmit a TP_IDL message throughout the test.

Test #14.3.6: Link Fail Effect on the Receive Functions

Purpose: To verify that, while in the Link Test Fail state, receive functions are disabled and that the Link Test Pass state is properly entered when receiving data on the RD circuit.

References:

[1] IEEE Std 1802.3d-1993: Section 6.2.1.7, Test Case ID 1411.07.05
[2] IEEE Std 802.3™-2008: Section 14.2.1.7, Figure 14-6

Resource Requirements:

- Packet Capture/Analysis Tool
- Arbitrary Waveform Generator
- Balun

Last Modification: September 6, 1996

Discussion:

For a signal to be accepted there needs to be a link present between the two stations. A link is recognized by the reception of link test pulses or data on a station's RD circuit; else the station enters the Link Test Fail state. When in this state, a valid packet sent to the RD circuit shall not be accepted, but shall cause the station to enter the Link Test Pass state. Thus, a packet immediately following the first packet shall then be accepted. An important exception to this is if the device performs auto-negotiation. As referenced in section 28.2.2.2 and figure 28-17, an auto-negotiating device will not transition to the Link Test Pass state when receiving 10BASE-T data.

Test Setup: See Figure 14.2.2-1.

Procedure:

1. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
2. Verify the Link Test Fail state by noticing TP_IDL on the TD circuit.
3. Send a single packet to the RD circuit of the DUT.
4. Verify that the packet was not accepted by the DUT.
5. Force the RD circuit to enter the Link Test Fail state by stopping any input on the RD circuit for 150 ms or more.
6. Verify the Link Test Fail state by noticing TP_IDL on the TD circuit.
7. Send two packets with an interframe gap of 9.6 μs to the RD circuit of the DUT.
8. Verify that the second packet was accepted by the DUT.

Observable Results:

- The DUT shall not accept the packet, as it is in the Link Test Fail state. In the series of two packets, the DUT shall not accept the first packet. If the device is not auto-negotiating it shall enter the Link Test Pass state because of RD_input.
- The DUT shall not accept the first packet in the series of two packets, but shall accept the second only if it is not a Clause 28-compliant, auto-negotiating device.

Appendix A: Test Equipment

AWG

An arbitrary waveform generator which matches the specifications in IEEE Std 1802.3d-1993 Section 6.3.4.4 with the exception that the sample resolution shall be 4 ns/point

BAL

100 Ω to 50 Ω balun impedance adapter as defined in IEEE Std 1802.3d-1993 Section 6.3.3.3

Current Probe

Meets specifications defined in IEEE Std 1802.3d-1993 Section 6.3.4.11

Oscilloscope

A digitizing signal analyzer which matches the specifications for an oscilloscope as defined in IEEE Std 1802.3d-1993 Section 6.3.4.8

Differential Voltage Probe

Meets specifications defined in IEEE Std 1802.3d-1993 Section 6.3.4.9

TP Test Card

A testing card with an RJ-45 interface containing the following options:

- Cross over at the input
- Cable termination with 100 Ω load, Test Load 1, or Test Load 2 (as defined in IEEE 802.3 Section 14.3.1.2.1 and Figure 14-11)
- Unshielded twisted pair model for 10BASE-T and 10BASE-Te (as defined in IEEE Std 802.3 Section 14.3.1.2)
- Link test pulse generator

Appendix B: References

ANSI/IEEE Std 802.3 2008, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

IEEE Std 1802.3d-1993, CSMA/CD Access Method and Physical Layer Specifications, Type 10BASE-T Medium Attachment Unit (MAU) Conformance Test Methodology (Section 6), May 5, 1994