ASPLOS-2023 : FIRST FIRESIM AND CHIPYARD CONFERENCE

CHIPSHOP

A Cloud-Based GUI for Accelerating SoC Design

sispace.tech/chipshop

CHIPSHOP

AGENDA

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Web based SoC Generation

FPGA Mapping and Bitstream Generation

Blackbox (IP) Integration

Real-time Collaboration and Version Control

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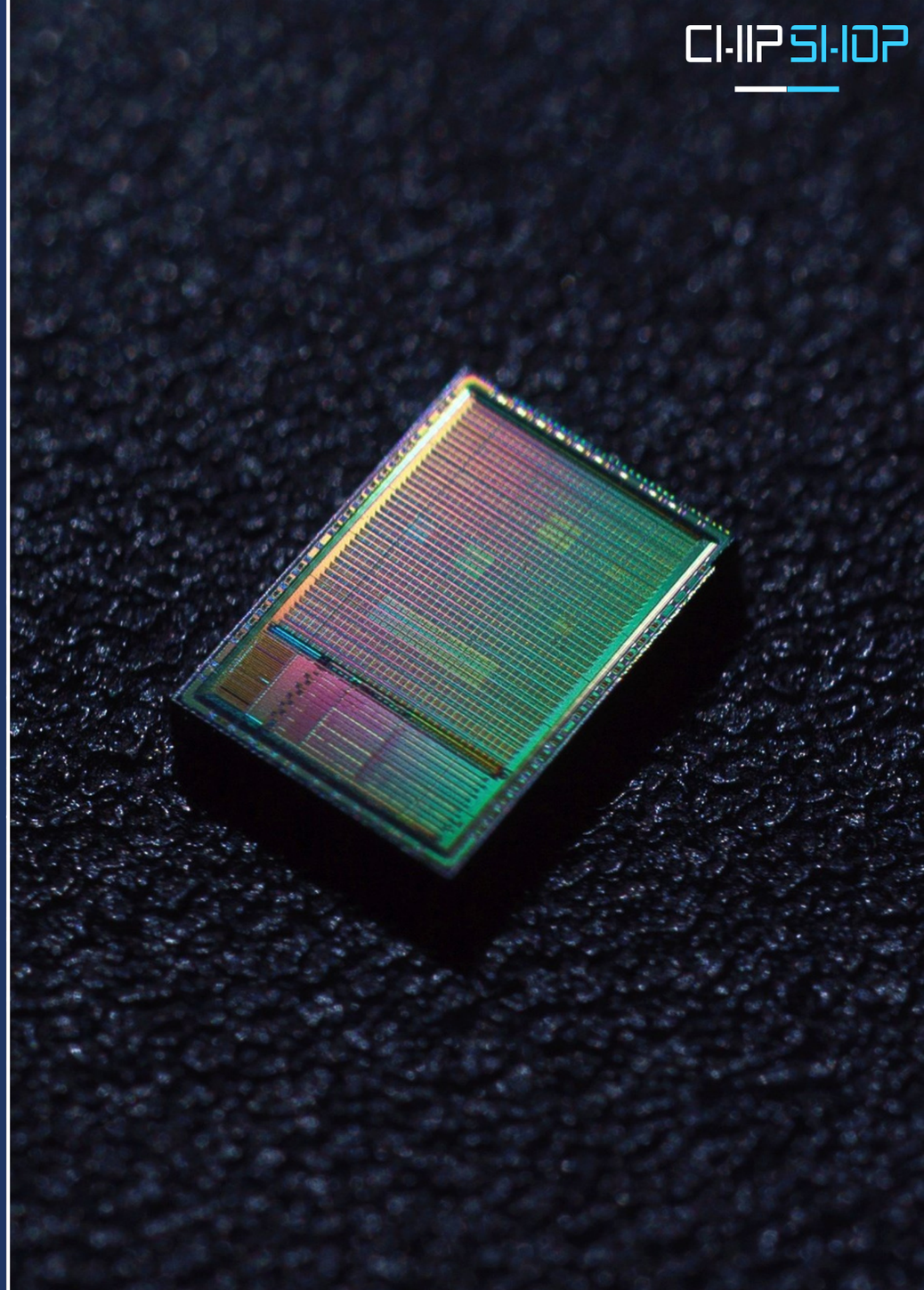
INTRODUCTION

PROBLEM STATEMENT

- Designing a System-on-Chip (SoC) is out of reach due to the high level of technical expertise required.
- It stifles innovation and advancement in the industry.
- Need for auser-friendly approach to SoC design.
- To make the design process easier and more efficient.
- In addition, it should democratise access to SoC design by making it broadly available to individuals without deep technical knowledge.
- This issue is already resolved by Chipyard, however using it and creating customised SoCs with it takes more technical know-how, making it only useful for a some specified users.



INTRODUCTION

CHIPSHOP

- ChipShop, a web-based GUI built on top of Chipyard.
- It enables users to configure and accelerate the SoC generation.
- Easy-to-use interface for Chipyard configuration.
- Streamlines the SoC design process and makes it accessible to a broader range of users.
- Addition of new IPs and automatic blackbox generation and integration for user-provided RTLs.
- Well-suited for large teams working on complex designs

CHIPSHOP

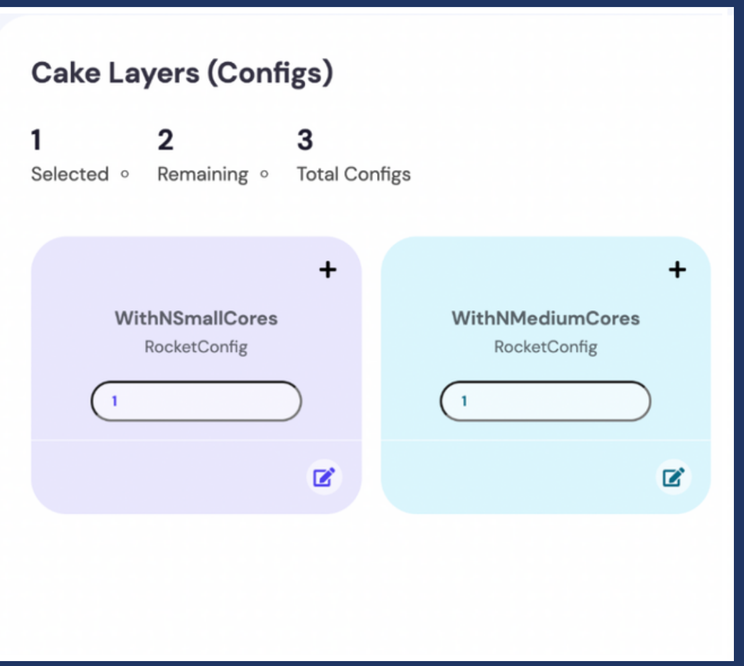
FEATURES

- Web based SoC Configuration
- FPGA Mapping and Bitstream Generation
- Blackbox (IP) Integration
- Real-time Collaboration and Version Control

CHIPSHOP

FEATURES

WEB BASED SOC CONFIGURATION



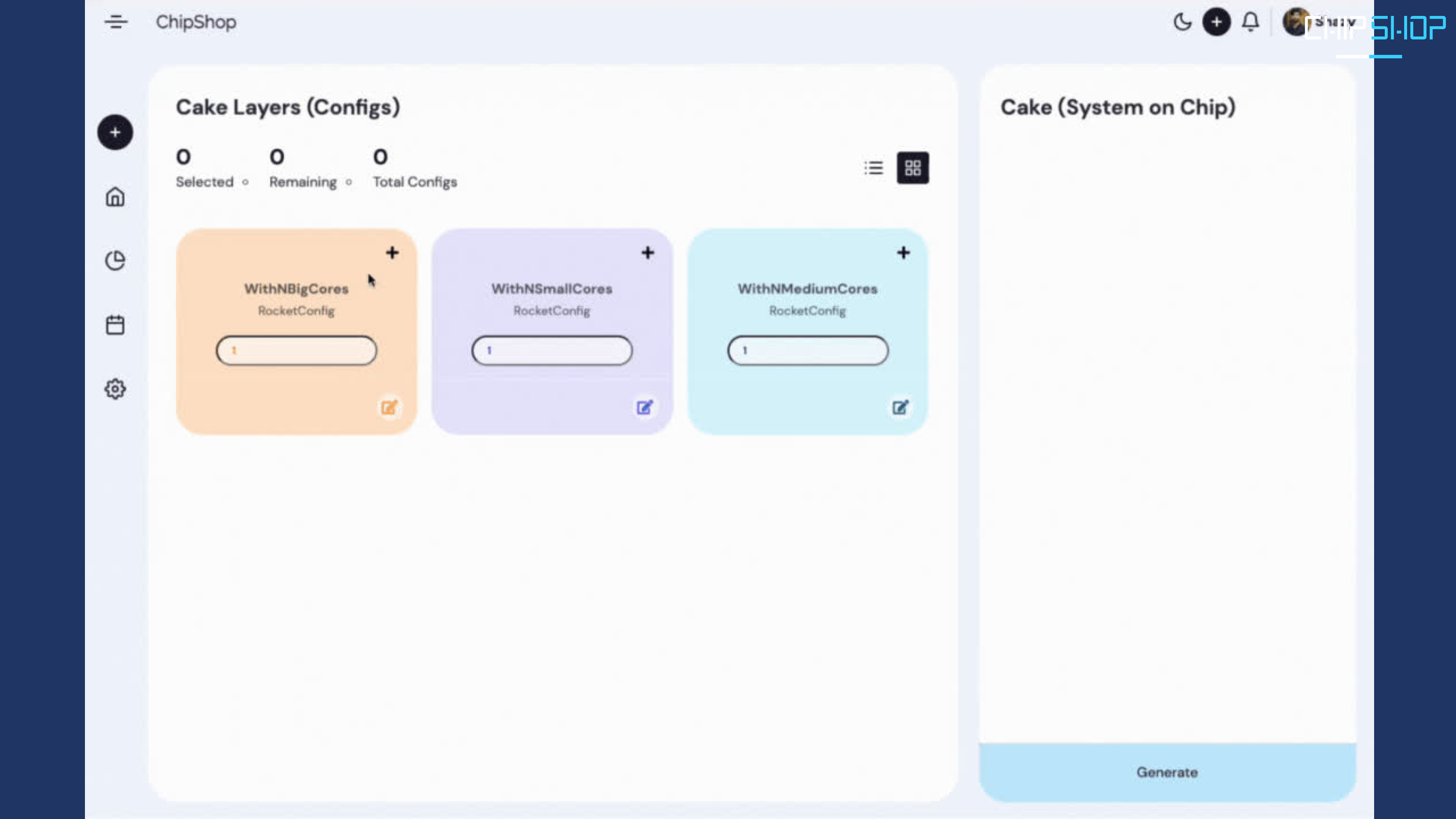
System-on-Chip (SoC) Configuration is done on the basis of Chipyard Cake Pattern. Users can add, remove, and edit cake layers (configs) to create a customised SoC.

Adding Cake Layers (Configs)

All the Configuration classes (Cake layers) can be added to create a custom System-on-Chip (SoC)

Editing Parameters for all Cake layers

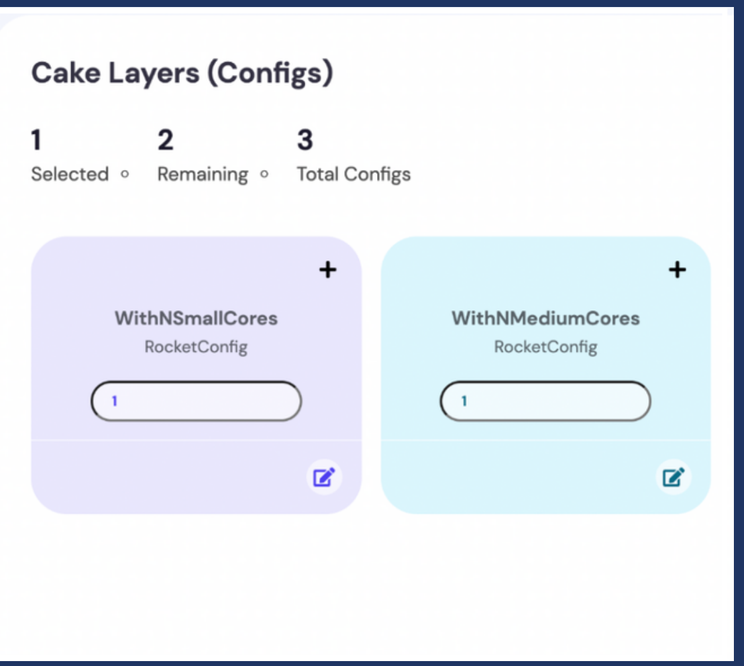
In addition, the parameters of those Configuration classes (Cake layers) can also be edited (customised)


ChipShop
Cake Layers (Configs)
0
Selected
0
Remaining
0
Total Configs
WithNBigCores
RocketConfig
1
WithNSmallCores
RocketConfig
1
WithNMediumCores
RocketConfig
1
Cake (System on Chip)
Generate

CHIPSHOP

FEATURES

FPGA MAPPING AND BITSTREAM GENERATION



ChipShop also offers Bitstream Generation of the generated SoC , along with mapping its I/Os onto FPGA components.

FPGA Target Selection

Users can select FPGA target from the available targets to generate bitstream for it

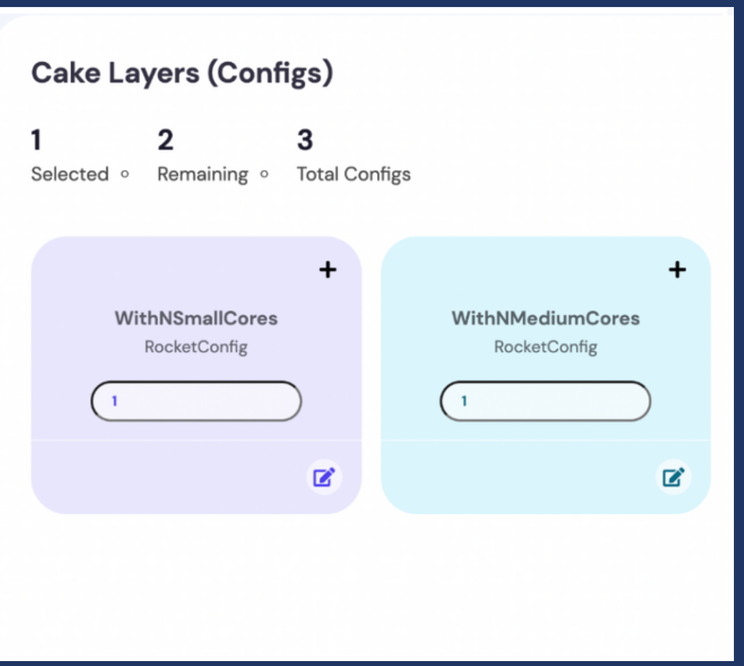
Mapping I/Os onto FPGA Components

In addition, the I/Os of the SoC like UART, SPI more custom IP I/Os can be mapped onto FPGA components

CHIPSHOP

FEATURES

REAL-TIME COLLABORATION AND VERSION CONTROL



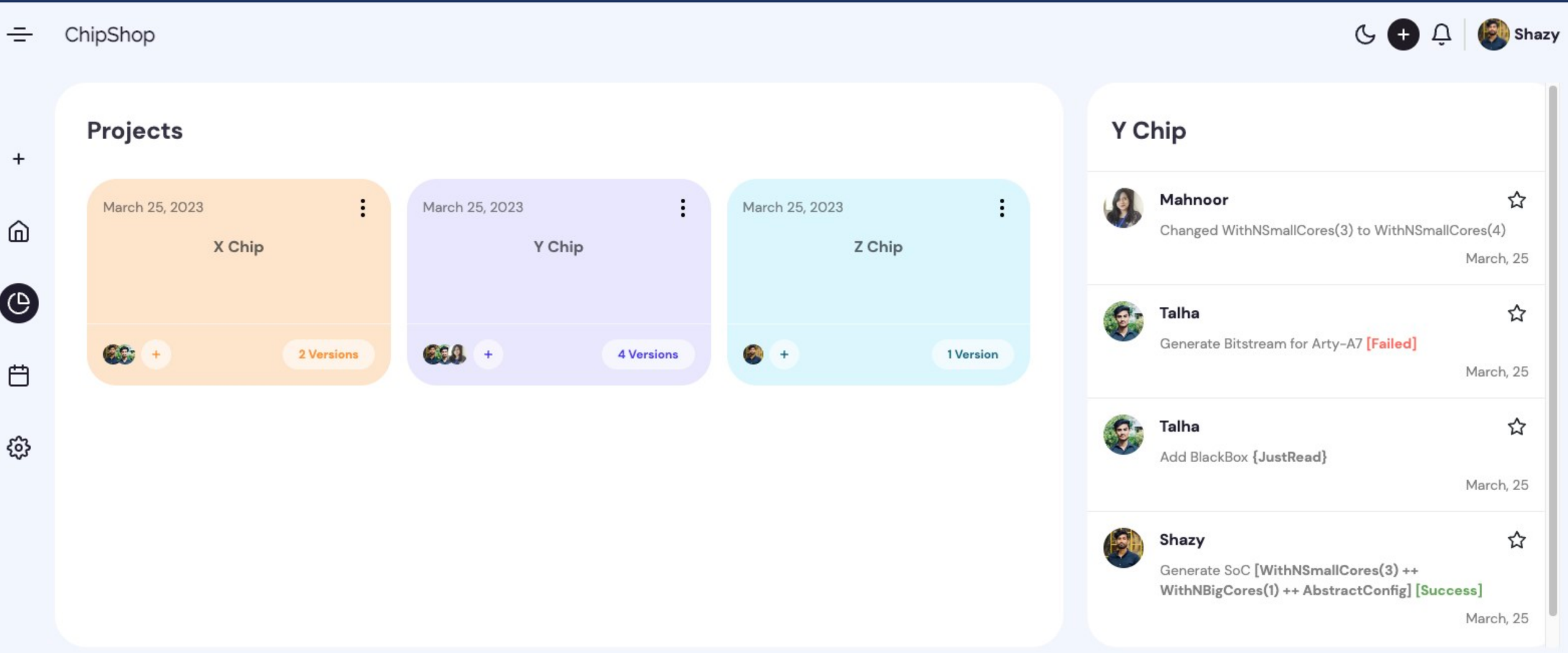
ChipShop also offers the feature of Real Time Collaboration and Version Control for each of the SoC Projects users create.

Share you SoC Project with others

Users can share their SoC Project with other Users, registered in ChipShop Workspace.

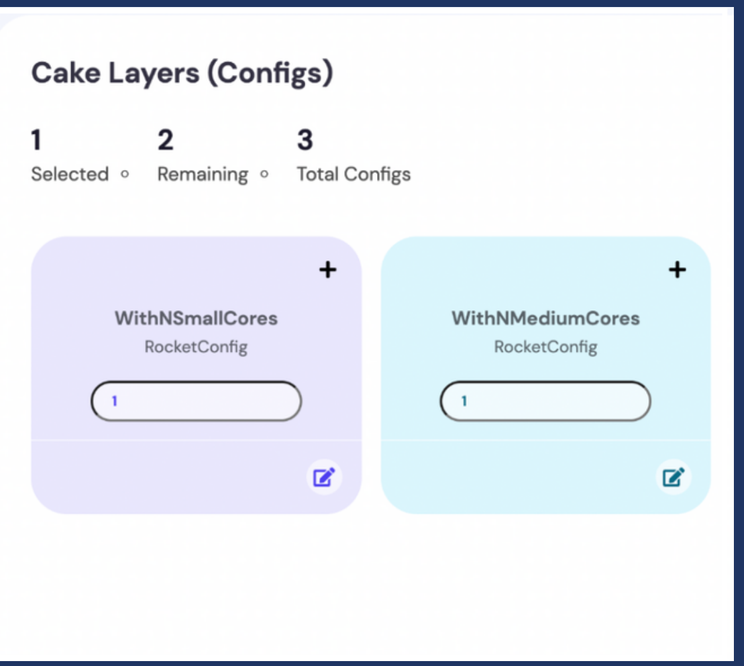
Version maintained history of changes

For every small change made by each user on a single project, after SoC Generation. Version based history is maintained.


ChipShop
Shazy
Projects
March 25, 2023
X Chip
2 Versions
March 25, 2023
Y Chip
4 Versions
March 25, 2023
Z Chip
1 Version
Y Chip
Mahnoor
Changed WithNSmallCores(3) to WithNSmallCores(4)
March, 25
Talha
Generate Bitstream for Arty-A7 [Failed]
March, 25
Talha
Add BlackBox {JustRead}
March, 25
Shazy
Generate SoC [WithNSmallCores(3) ++ WithNBigCores(1) ++ AbstractConfig] [Success]
March, 25

FEATURES

BLACKBOX (IP) INTEGRATION



Users can also attach their own Custom IPs with the System on Chip as an Memory Mapped Input Output (MMIO).

Integrate IP in the SoC Address Space

ChipShop features quick and easy integration of User IP into the SoC Address Space, at user's defined custom address.

Map the IP's I/Os to FPGA via ChipTop

The I/Os of the IP can be routed to ChipTop in order to be mapped onto FPGA.

ChipShop

Cake Layers (Configs)

0 Selected ◦ 0 Remaining ◦ 0 Total Configs

Add BlackBox / Custom IP

WithNBigCores
RocketConfig
1

WithNSmallCores
RocketConfig
1

WithNMediumCores
RocketConfig
1

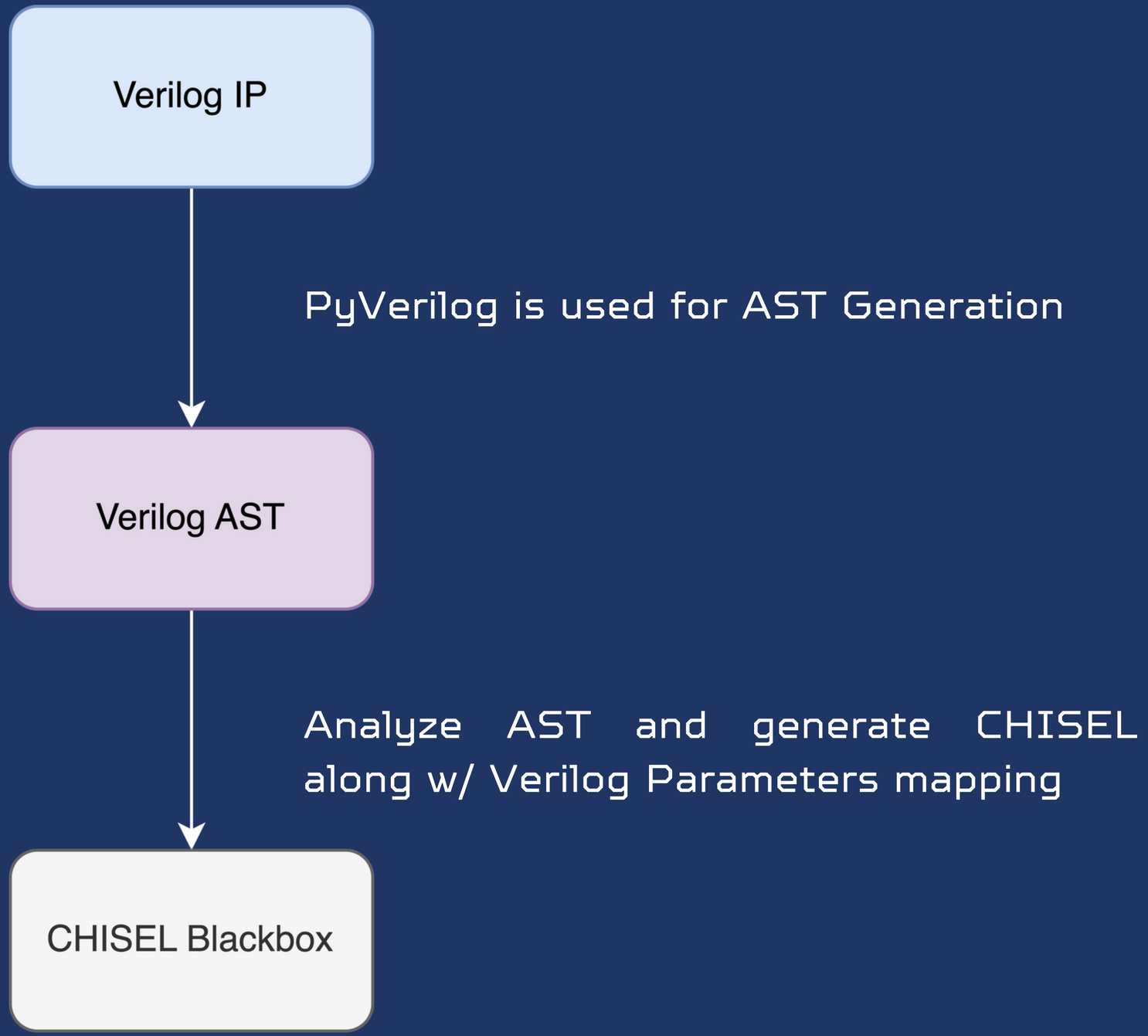
Cake (System on Chip)

Generate

FEATURES

chiV: CHISEL INTERFACING FOR VERILOG IPs

In addition to the Blackbox Integration feature, we have created a utility software for Interfacing of Verilog IPs into CHISEL HDL.


Verilog IP
PyVerilog is used for AST Generation
Verilog AST
Analyze AST and generate CHISEL
along w/ Verilog Parameters mapping
CHISEL Blackbox

Technical

APPLICATIONS

- Custom SoC design for specialized applications (IoT, automotive, aerispace).
- Educational purposes: learning tool to teach SoC design concepts to students.
- Rapid prototyping and testing of SoC designs
- Startups or small companies.
- Large organizations that want to accelerate the SoC design.

TECH STACK

- CHISEL
- Scala
- Python
- DJANGO-REST
- REACT
- Docker

CHIPSHOP

ChipShop Team

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Conclusion

FUTURE WORK

- To extend support for FireSim.
- Additionally, to expand Bitstream Generation support using open-source tools.
- Add more targets for FPGA Platforms.

THANK YOU

Any Questions?

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