FireSim

Project Management, Contributing & Conclusion

FireSim Intensive
Chisel Community Conference 2018
Speaker: David Biancolin

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Development Model – Branches

- FireSim and its key submodules (FireChip, MIDAS, aws-fpga) have two write-controlled branches

- master
  - Stable
  - Contains the most recent release of FireSim
  - Can replicate ISCA2018 paper results

- dev
  - Main development branch
  - Base branch for feature PRs and non-critical bug fixes
  - Every merge commit has globally shared, regenerated AGFIs

Development Model – Merges & Releases

- To merge a feature branch into dev:
  - Pass all MIDAS-level tests (in sim/: `make test`)
  - Regenerate all AGFIs if RTL changes were made
  - Associated submodule PRs should be merged; submodule pointers should point at merge commit on dev
- Changes to dev will be summarized in a "Dev-tracking PR"
  - PR description will become the Changelog entry
- Dev will be periodically merged into master and tagged as a release
  - Changelog will be updated
  - Submodule dev branches will also be merged into master

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How to Get Help

- FireSim and MIDAS adds a bunch of additional complexity on top of Rocket-Chip, Chisel, FIRRTL, Scala…
  - But there's a team of us here to help!
- For general questions:
  - Post on the google groups: https://groups.google.com/forum/#!forum/firesim
  - Check out the docs: https://docs.fires.im/en/latest/
  - (Nascent) FAQ section: https://docs.fires.im/en/latest/Advanced-Usage/FAQs.html

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Reporting Issues

- If you think you've encountered a bug (in FireSim or MIDAS):
  - Open an issue on FireSim's github page
- Try your best to open an issue in the most relevant repo
  - Please don't open duplicates across multiple repos!
  - If you are unsure, default to FireSim and we'll be happy to redirect you

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Contributing

- We welcome PRs!
- Issues are labeled with "Good First Issue"
- Ask on the google groups for suggestions

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Regarding Future Work

- There are many research projects underway at UCB-BAR using and improving FireSim

- Many will be merged into mainline FireSim

- There will be API breakages -> We apologize in advance
  - Watch the changelogs, dev tracking PRs

Our goal: make FireSim the standard open way to do fast full-system simulation of Chisel-designed systems, especially ones based on Rocket-Chip.

Focus on:

- Generality (eg. support multi-clock target designs)

- Robustness (eg. More extensive testing in RTL-simulation; CI; regressions)

- Debuggability (eg. DESSERT features)

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Conclusion

Key links:
- Website: https://fires.im
- Google Groups: https://groups.google.com/forum/#!forum/firesim
- Docs: https://docs.fires.im/en/latest/
- Twitter: @firesimproject

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