BK3268 Bluetooth Audio MCU+DSP Dual Core SoC

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Revision History

Rev.	Date	Remark
0.1	7/Mar/2018	Initial version
0.2	24/May/2018	Update package definition, only VDD3IOFLA-pin position is changed
0.3	18/July/2018	BK3268 Production version. Add 6X6-QFN48 package and 7x7-QFN56 package. Add GPIO16-GPIO26 definition. Update download port from GPIO0/GPIO1 to GPIO6/GPIO7.
0.4	26/July/2018	Add ANC package information and related function description
0.5	14/Aug/2018	Update electrical parameter.

Contents

1. General Description

The BK3268 is a low power Bluetooth classic and low energy 5.0 version system on chip (SoC) audio device. It integrates a 32-bit MCU and a 32-bit TL420 DSP; both have their own instruction memory and their own data memory. It has UART, I2C, SPI, IrDA, SDIO, I2S and USB interface. It has also QSPI interface for data memory and FLASH extension. Two sets of digital microphone interface support up to four digital microphone.

The BK3268 provides up to 6 channel PWM output. The ADC supports eight channels from GPIO and three internal channels from USB power, temperature sensor and battery input.

The BK3268 has strong audio peripheral such as dual channel analog microphone input, dual channel line in input, and dual channel stereo output. All these peripherals have DMA channel to and from memory.

The device incorporates on-chip power management with linear and switch-mode buck regulators and also includes a 220 mA internal battery charge controller to further reduce external bill of material (BOM) costs.

2. Features

- Operating from 2.8 V to 4.2 V
- Bluetooth 5.0 classic and low energy
- -93 dBm sensitivity and 8 dBm output power
- 120 MHz 32-bit MCU
- 180 MHz 32-bit TL420 DSP
- Hardware mailbox communication between MCU and DSP
- 96 KB share memory
- Up to 272 KB total data memory
- 24 bits and 104 dB SNR stereo DAC
- Dual microphone and stereo line in
- 9 mA average current for A2DP
- 300 uA sniff current
- 0.8 uA deep sleep current
- A2DP v1.3, AVRCP v1.6, HFP v1.7, HID v1.1, AVCTP v1.4, AVDTP v1.3, and SPP v1.2
- Two sets of digital microphone interface
- Two wires UART download interface
- QSPI for external SPI RAM/FLASH
- SPI, UART, I2C, SDIO and USB
- I2S interface with MCLK output
- Interface for external PA and LNA
- 220 mA battery charge controller
- 32 Byte eFUSE

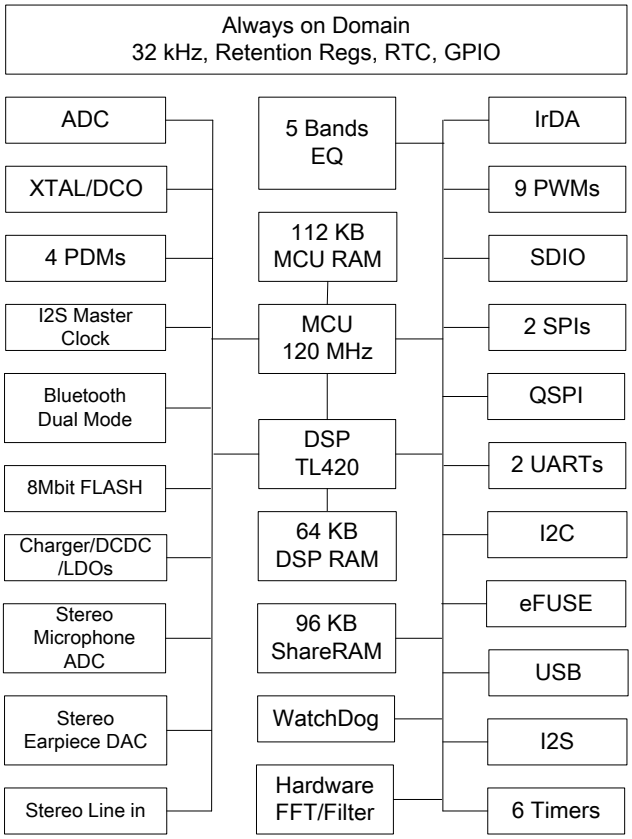


Figure 1 Block diagram of BK3268

3. Pin Definition

The BK3268 is available in 40-pin 5x5 mm^2 QFN package, 48-pin 6x6 mm^2 QFN and 56-pin 7x7 mm^2 QFN package.

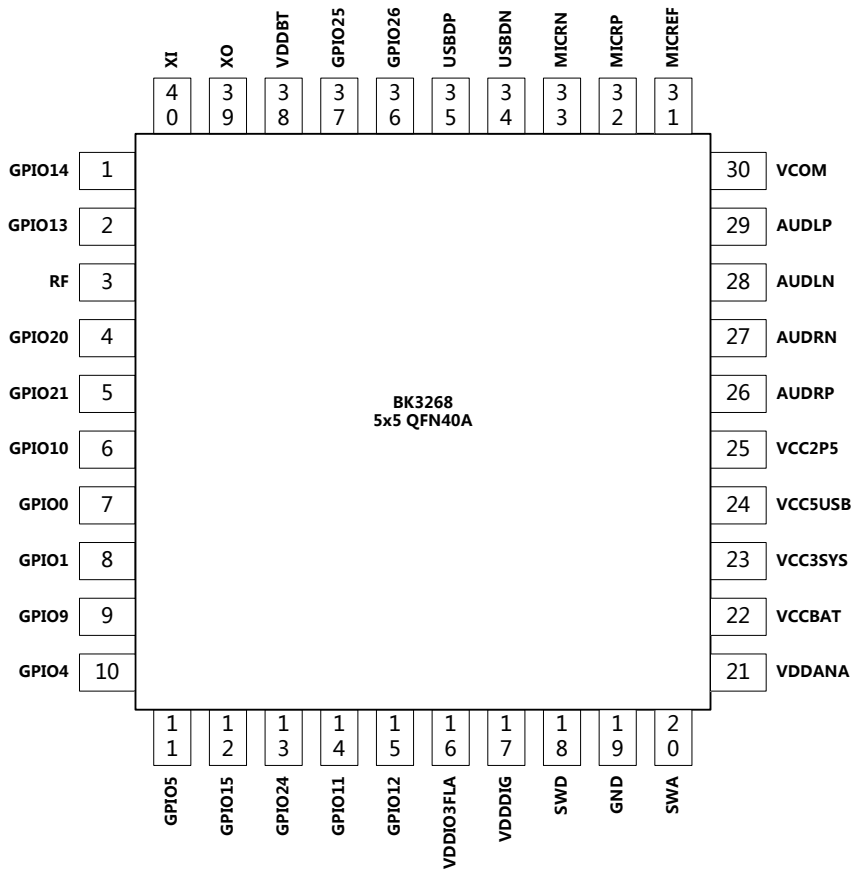


Figure 2 QFN40A Package

Pin Description of QFN40A Package		
PIN	**Name**	**Description**
1	GPIO14	GPIO14, JTAG_TDO/PWM5/ADC7/PCM_DOUT
2	GPIO13	GPIO13, JTAG_TDI/PWM4/ADC6/PCM_DIN/SD_DATA0/SPI2_MISO
3	RF	RF port
4	GPIO20	GPIO20, SD_DATA1/DMIC1_DAT
5	GPIO21	GPIO21, SD_DATA2/DMIC1_CLK
6	GPIO10	GPIO10, SD_DATA0/RX_EN/SPI2_MISO
7	GPIO0	GPIO0, UART_TXD/I2C_SCL
8	GPIO1	GPIO1, UART_RXD/I2C_SDA
9	GPIO9	GPIO9, SD_CMD/TX_EN/SPI2_MOSI
10	GPIO4	GPIO4, SPI_MOSI//I2C_SCL

11	GPIO5	GPIO5, SPI_MOSI//I2C_SCL
12	GPIO15	GPIO15, ADC10
13	GPIO24	GPIO24, CLKOUT2
14	GPIO11	GPIO11, JTAG_TCK/PWM2/ADC4/PCM_SYNC/SD_CLK//SPI2_SCK
15	GPIO12	GPIO12, JTAG_TMS/PWM3/PCM_CLK/SD_CMD/SPI2_MOSI
16	VDDIO3VFLA	FLASH power supply
17	VDDDIG	Digital LDO output
18	SWD	Buck component
19	GND	Ground
20	SWA	Buck component
21	VDDANA	Analog LDO output
22	VCCBAT	Battery input
23	VCC3SYS	System LDO output
24	VCC5USB	USB charge power input
25	VCC2P5	Power supply for eFUSE write
26	AUDRP	Audio right channel positive
27	AUDRN	Audio right channel negative
28	AUDLN	Audio left channel negative
29	AUDLP	Audio left channel positive
30	VCOM	Common mode voltage for audio output
31	MICREF	Microphone reference voltage
32	MICRP	Microphone input positive
33	MICRN	Microphone input negative
34	USBDN	GPIO7, PWM1, Download port
35	USBDP	GPIO6, PWM0, Download port
36	GPIO26	GPIO26, DMIC2_CLK
37	GPIO25	GPIO25, DMIC2_DAT
38	VDDBT	Bluetooth RF LDO output
39	XO	Crystal output
40	XI	Crystal input

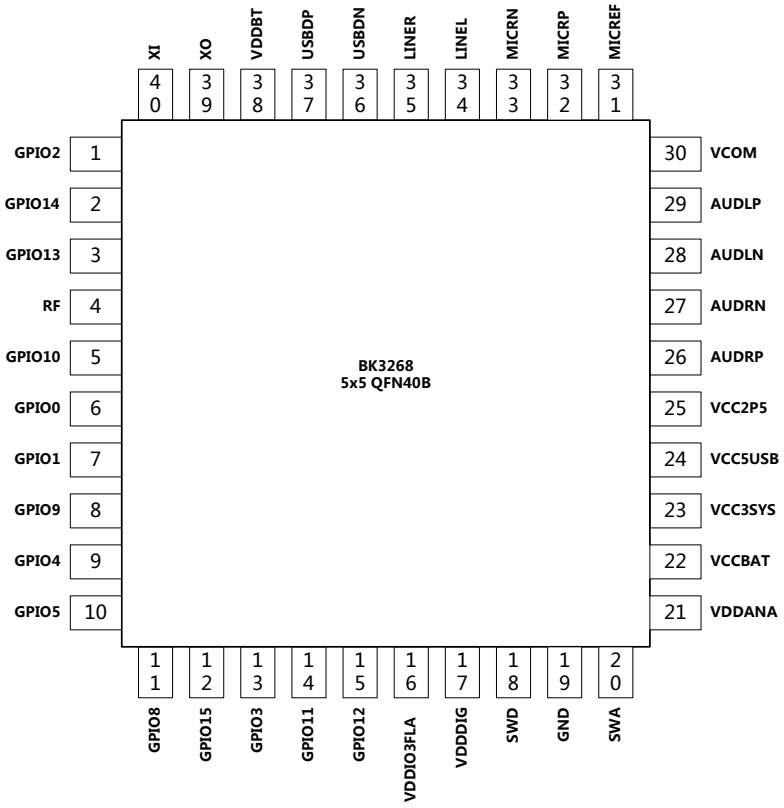


Figure 3 QFN40B Package

Pin Description of QFN40B Package		
PIN	**Name**	**Description**
1	GPIO2	GPIO2, SPI_CSN/ADC1/IrDA/Capture Time
2	GPIO14	GPIO14, JTAG_TDO/PWM5/ADC7/PCM_DOUT
3	GPIO13	GPIO13, JTAG_TDI/PWM4/ADC6/PCM_DIN/SD_DATA0/SPI2_MISO
4	RF	RF port
5	GPIO10	GPIO10, SD_DATA0/RX_EN/SPI2_MISO
6	GPIO0	GPIO0, UART_TXD/I2C_SCL
7	GPIO1	GPIO1, UART_RXD/I2C_SDA
8	GPIO9	GPIO9, SD_CMD/TX_EN/SPI2_MOSI
9	GPIO4	GPIO4, SPI_MOSI//I2C_SCL
10	GPIO5	GPIO5, SPI_MOSI//I2C_SCL
11	GPIO8	GPIO8, SD_CLK//SPI2_SCK

12	GPIO15	GPIO15, ADC10
13	GPIO3	GPIO3, SPI_SCK/CLKOUT
14	GPIO11	GPIO11, JTAG_TCK/PWM2/ADC4/PCM_SYNC/SD_CLK//SPI2_SCK
15	GPIO12	GPIO12, JTAG_TMS/PWM3/PCM_CLK/SD_CMD/SPI2_MOSI
16	VDDIO3VFLA	FLASH power supply
17	VDDDIG	Digital LDO output
18	SWD	Buck component
19	GND	Ground
20	SWA	Buck component
21	VDDANA	Analog LDO output
22	VCCBAT	Battery input
23	VCC3SYS	System LDO output
24	VCC5USB	USB charge power input
25	VCC2P5	Power supply for eFUSE write
26	AUDRP	Audio right channel positive
27	AUDRN	Audio right channel negative
28	AUDLN	Audio left channel negative
29	AUDLP	Audio left channel positive
30	VCOM	Common mode voltage for audio output
31	MICREF	Microphone reference voltage
32	MICRP	Microphone input positive
33	MICRN	Microphone input negative
34	LINEL	Line left channel input
35	LINER	Line right channel input
36	USBDN	GPIO7, PWM1, Download port
37	USBDP	GPIO6, PWM0, Download port
38	VDDBT	Bluetooth RF LDO output
39	XO	Crystal output
40	XI	Crystal input

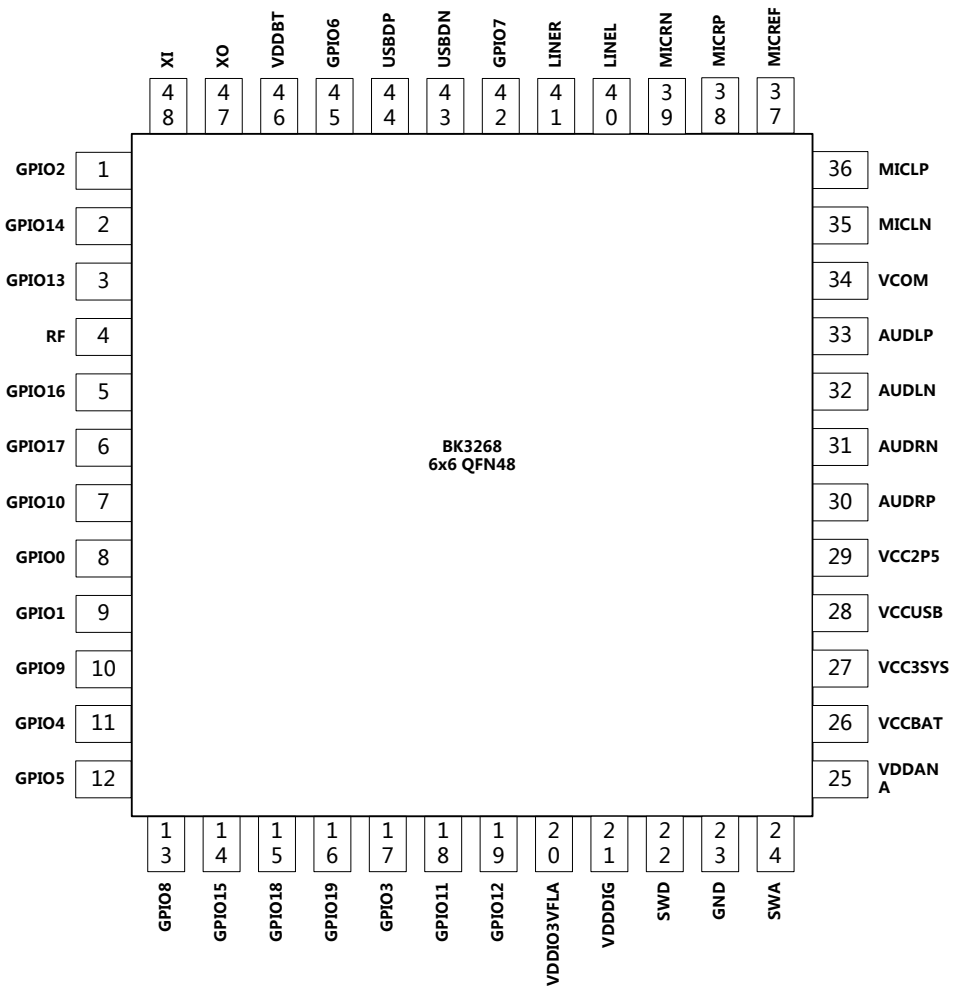


Figure 4 QFN48 Package

Pin Description of 48-Pin Package		
PIN	**Name**	**Description**
1	GPIO2	GPIO2, SPI_CSN/ADC1/IrDA/Capture Time
2	GPIO14	GPIO14, JTAG_TDO/PWM5/ADC7/PCM_DOUT
3	GPIO13	GPIO13, JTAG_TDI/PWM4/ADC6/PCM_DIN/SD_DATA0/SPI2_MISO
4	RF	RF port
5	GPIO16	GPIO16, TX_EN/UART2_TXD
6	GPIO17	GPIO17, RX_EN/UART2_RXD
7	GPIO10	GPIO10, SD_DATA0/RX_EN/SPI2_MISO

8	GPIO0	GPIO0, UART_TXD/I2C_SCL, Download port
9	GPIO1	GPIO1, UART_RXD/I2C_SDA, Download port
10	GPIO9	GPIO9, SD_CMD/TX_EN/SPI2_MOSI
11	GPIO4	GPIO4, SPI_MOSI//I2C_SCL
12	GPIO5	GPIO5, SPI_MOSI//I2C_SCL
13	GPIO8	GPIO8, SD_CLK//SPI2_SCK
14	GPIO15	GPIO15,ADC10
15	GPIO18	GPIO18, PWM6
16	GPIO19	GPIO19, PWM7/ADC2
17	GPIO3	GPIO3, SPI_SCK/CLKOUT
18	GPIO11	GPIO11, JTAG_TCK/PWM2/ADC4/PCM_SYNC/SD_CLK//SPI2_SCK
19	GPIO12	GPIO12, JTAG_TMS/PWM3/PCM_CLK/SD_CMD/SPI2_MOSI
20	VDDIO3VFLA	FLASH power supply
21	VDDDIG	Digital LDO output
22	SWD	Buck component
23	GND	Ground
24	SWA	Buck component
25	VDDANA	Analog LDO output
26	VCCBAT	Battery input
27	VCC3SYS	System LDO output
28	VCC5USB	USB charge power input
29	VCC2P5	Power supply for eFUSE write
30	AUDRP	Audio right channel positive
31	AUDRN	Audio right channel negative
32	AUDLN	Audio left channel negative
33	AUDLP	Audio left channel positive
34	VCOM	Common mode voltage for audio output
35	MICLN	Microphone left channel input negative
36	MICLP	Microphone left channel input positive
37	MICREF	Microphone reference voltage
38	MICRP	Microphone right channel input positive
39	MICRN	Microphone right channel input negative
40	LINEL	Line left channel input

41	LINER	Line right channel input
42	GPIO7	GPIO7，PWM1/UART_RXD，Download port
43	USBDN	GPIO7, PWM1
44	USBDP	GPIO6, PWM0
45	GPIO6	GPIO6，PWM0/UART_TXD，Download port
46	VDDBT	Bluetooth RF LDO output
47	XO	Crystal output
48	XI	Crystal input

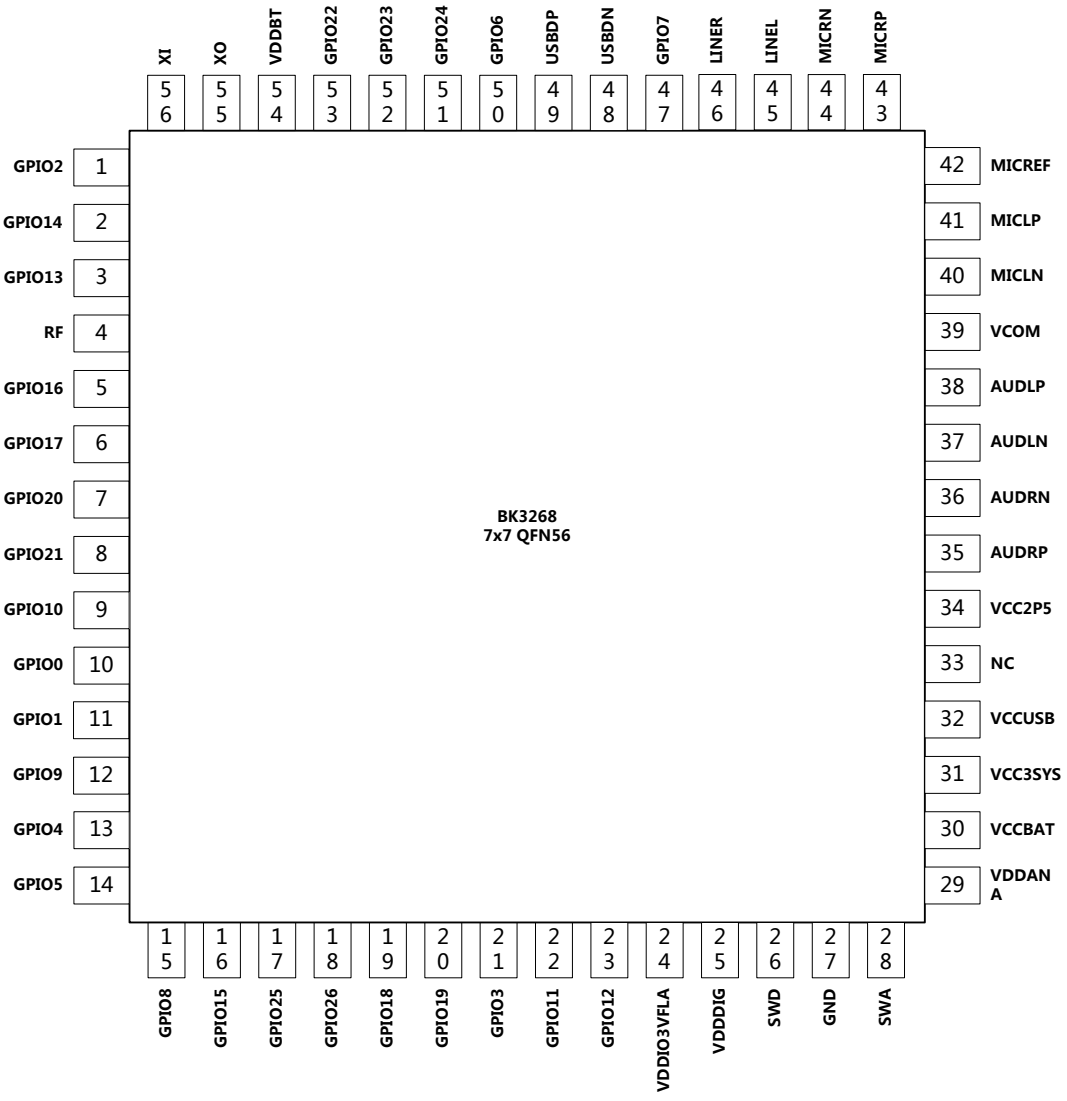


Figure 5 QFN56 Package

Pin Description of 56-Pin Package		
PIN	**Name**	**Description**
1	GPIO2	GPIO2, SPI_CSN/ADC1/IrDA/Capture Time
2	GPIO14	GPIO14, JTAG_TDO/PWM5/ADC7/PCM_DOUT
3	GPIO13	GPIO13, JTAG_TDI/PWM4/ADC6/PCM_DIN/SD_DATA0/SPI2_MISO
4	RF	RF port
5	GPIO16	GPIO16, TX_EN/UART2_TXD
6	GPIO17	GPIO17, RX_EN/UART2_RXD
7	GPIO20	GPIO20，SD_DATA1/DMIC**1**_DAT
8	GPIO21	GPIO21，SD_DATA2/DMIC**1**_CLK
9	GPIO10	GPIO10, SD_DATA0/RX_EN/SPI2_MISO
10	GPIO0	GPIO0, UART_TXD/I2C_SCL
11	GPIO1	GPIO1, UART_RXD/I2C_SDA
12	GPIO9	GPIO9, SD_CMD/TX_EN/SPI2_MOSI
13	GPIO4	GPIO4, SPI_MOSI/I2C_SCL
14	GPIO5	GPIO5, SPI_MOSI/I2C_SCL
15	GPIO8	GPIO8, SD_CLK/SPI2_SCK
16	GPIO15	GPIO15, ADC10
17	GPIO25	GPIO25，DMIC**2**_DAT/ADC8
18	GPIO26	GPIO26，DMIC**2**_CLK/ADC9
19	GPIO18	GPIO18, PWM6
20	GPIO19	GPIO19, PWM7/ADC2
21	GPIO3	GPIO3, SPI_SCK/CLKOUT
22	GPIO11	GPIO11, JTAG_TCK/PWM2/ADC4/PCM_SYNC/SD_CLK//SPI2_SCK
23	GPIO12	GPIO12, JTAG_TMS/PWM3/PCM_CLK/SD_CMD/SPI2_MOSI
24	VDDIO3VFLA	FLASH power supply
25	VDDDIG	Digital LDO output
26	SWD	Buck component
27	GND	Ground
28	SWA	Buck component
29	VDDANA	Analog LDO output

30	VCCBAT	Battery input
31	VCC3SYS	System LDO output
32	VCC5USB	USB charge power input
33	NC	No connection
34	VCC2P5	Power supply for eFUSE write
35	AUDRP	Audio right channel positive
36	AUDRN	Audio right channel negative
37	AUDLN	Audio left channel negative
38	AUDLP	Audio left channel positive
39	VCOM	Common mode voltage for audio output
40	MICLN	Microphone left channel input negative
41	MICLP	Microphone left channel input positive
42	MICREF	Microphone reference voltage
43	MICRP	Microphone right channel input positive
44	MICRN	Microphone right channel input negative
45	LINEL	Line left channel input
46	LINER	Line right channel input
47	GPIO7	GPIO7，PWM1/UART_RXD，Download port
48	USBDN	GPIO7, PWM1
49	USBDP	GPIO6, PWM0
50	GPIO6	GPIO6，PWM0/UART_TXD，Download port
51	GPIO24	GPIO24，CLKOUT2
52	GPIO23	GPIO23，CLK32K_Input/PWM8
53	GPIO22	GPIO22，SD_DATA3
54	VDDBT	Bluetooth RF LDO output
55	XO	Crystal output
56	XI	Crystal input

4. Functional Description

4.1. Clock

There are five clock types in the BK3268.

High frequency crystal: 26 MHz crystal is required, and there is tunable load capacitance from 6 to 18 pF (both side have this capacitance) with 64 steps to tune the crystal frequency, that no external capacitance is needed.

Two internal digital control oscillators (DCO): The DCO for MCU has tunable frequency from 26 MHz to 120 MHz, and the DCO for DSP has tunable frequency up to 180 MHz.

Internal 32 KHz ring oscillator: The low power ring oscillator has frequency around 32 kHz, which is normally used for timer in sleep mode.

32 kHz clock divided from crystal: This accurate 32 kHz clock is mainly used by Bluetooth sniff mode, to wake up receiver at constant interval.

Audio clock: The audio source clock can be either from high frequency crystal or audio digital PLL. To support high performance audio performance and I2S master clock output, the audio clock should be derived from audio digital PLL.

4.2. Reset

System power on, digital power on and watch dog reset have the same reset effect, that any reset will reset the BK3268 whole chip to initial status.

Waking up from either shut down mode or deep sleep mode will power on digital from power down mode, that trigger the whole system reset procedure.

4.3. Power management

The BK3268 can be powered directly from a 2.8V to 4.2V external battery via the VCCBAT pin or it can be powered from a 4.75V to 5.75V USB power supply via the VCC5USB pin. The VCC5USB can be also used to charge battery with internal charge control circuit.

To reduce power, the BK3268 can be put in three low power modes as follows.

Shutdown – In this mode all circuits are powered down except for the GPIOX interface to allow external circuitry to wake-up the device. Software can enter this mode by write special register and system can only be waked up by active low level applied on GPIOX or VCC5USB low to high transition. (GPIOX: There are 5 channels to wake-up the device from shutdown mode, GPIO15 is one channel, and other four channels can be any GPIO from GPIO0 to GPIO26 by write special register)

Deep sleep mode – In this mode all circuits are powered down except the GPIO and RTC timer, that any GPIO edge transition or time out event can power up the system again. The VCC5USB low to high transition can also wake up MCU.

Standby – In this mode the MCU stop running and all peripheral interrupt can resume MCU.

4.4. Bluetooth

The BK3268 has both classic Bluetooth 2.1+EDR and Bluetooth low energy 4.2 component. Both the classic and BLE has their own independent clock and synchronization logic, that support simultaneously classic and BLE link much more efficient and stable.

4.5. Audio Peripherals

The BK3268 comes with a rich set of audio peripherals to enhance the Bluetooth listening experience. The chip includes a 5-band digital equalizer, 16 bits 96 dB signal-to-noise ratio (SNR) stereo analog-to-digital converter (ADC) and 24 bits 104 dB digital-to-analog converter (DAC), microphone input amplifier and bias, line-in input, and stereo audio left and right (L/R) outputs. The DAC is capable of driving 16 Ω speakers with up to 30 pF of load capacitance.

The typical sample rate of ADC and DAC is to 8 kHz、44.1 kHz and 48 kHz, but could be set to any number from 7.35 kHz to 96 kHz.

A dedicated 5-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption. The 5-band equalizer is easily configured using the BK3268 software configuration tool kit.

BK3268 includes stereo line-in inputs which connect to the stereo left and right channel ADCs through a 0~6 dB amplifier with 2 dB step. The digitized line-in inputs can be further processed with the 5-band equalizer prior to digital-to-analog conversion.

There is a hardware accelerator with the FFT and FIR mode, which can do either 256 points complex hardware FFT or dual channel 256 taps FIR filter. The operation speed can be same as MCU clock.

There are two sets of digital microphone interface to support up to 4 digital microphone. The PDM does the 8:1 CIC decimation that the PCM

sample rate could be up to 384 kHz when the PDM clock frequency is 3.072 MHz.

4.6. MCU and DSP

The BK3268 includes a 32-bit internal RISC MCU, memory and a DMA bus controller to run the Bluetooth software stack and application while supporting efficient execution and data exchange with the internal FLASH memory. The JTAG interface can be used for on-line debug and can also be configured as GPIO. The MCU runs directly from FLASH with internal cache. There are 112 KB dedicate data RAM and 96 KB share data RAM accessible by MCU.

There is a TL420 DSP to take signal processing task, but it can also access all the peripherals, and share 96 KB data memory with MCU. The DSP has dedicate 160 KB program RAM and 64 KB data RAM. The DSP can run with only internal 160 KB program and MCU is responsible load DSP program from FLASH to DSP program RAM. When the DSP code is larger than 160 KB, it can also set to run from FLASH with internal cache.

The whole DSP system including DSP core, 160 KB program RAM and 64 KB DSP data RAM could be power down while MCU is active to save power when DSP is not necessary.

The mailbox is used for communication between MCU and DSP. There are two group command and data registers in each direction, and interrupt register should be written after command and data are ready. After interrupted, the core can check the status register to know which group command and data is updated.

4.7. Data Memory Access

There are four data memory blocks accessible by the system.

- 112 KB tight couple data memory on the MCU core
- 64 KB tight couple data memory on the DSP core
- 96 KB share memory on the bus
- External PSRAM on the QSPI interface, directly mapping on the data memory address space

MCU, DSP and DMA can access all four data memory blocks. Tight couple memory has the fastest access speed for its owner core but also accessible by other host at cost of latency.

4.8. DMA

There DMA is used to transfer content between memory mapped device and the data memory. Total five DMA channels can work simultaneously, and two of them can be used by audio ADC and DAC with auto active function, which other three work once per MCU activation.

DMA can access I2S, audio ADC, audio DAC, PSRAM, digital microphone and UART interface.

4.9. GPIO

The BK3268 has total 27 GPIOs, which can be configured as either input or output, and the output drive capability can be programmed from 5mA to 32 mA. The GPIO voltage is constantly defined by VCC3SYS. Most of them

have peripheral mode or connected with analog function. The GPIO6 and GPIO7 pair are also used for UART download. The download mode is entered as long as the download port detected special command during short interval after the chip is reset to active mode, and after that time, all the download pin can be only used as GPIO and peripheral function.

GPIO	Peripheral Mode1	Peripheral Mode2	Peripheral Mode3	Peripheral Mode4	Peripheral Mode5
GPIO0	UART_TXD	I2C_SCL			
GPIO1	UART_RXD	I2C_SDA			
GPIO2	SPI_CSN	IrDA	CaptureTime		
GPIO3	SPI_SCK	CLKOUT			
GPIO4	SPI_MOSI	I2C_SCL			
GPIO5	SPI_MISO	I2C_SDA			
GPIO6	PWM0	UART_TXD			
GPIO7	PWM1	UART_RXD			
GPIO8	SD_CLK	SPI2_SCK			
GPIO9	SD_CMD	TX_EN	SPI2_MOSI		
GPIO10	SD_DATA0	RX_EN	SPI2_MISO		
GPIO11	JTAG_TCK	PWM2	SPI2_SCK	SD_CLK	PCM_SYNC
GPIO12	JTAG_TMS	PWM3	SPI2_MOSI	SD_CMD	PCM_CLK
GPIO13	JTAG_TDI	PWM4	SPI2_MISO	SD_DATA0	PCM_DIN
GPIO14	JTAG_TDO	PWM5			PCM_DOUT
GPIO15					
GPIO16	TX_EN	UART2_TXD			
GPIO17	RX_EN	UART2_RXD			
GPIO18	PWM6				
GPIO19	PWM7				
GPIO20	SD_DATA1	DMIC**1**_DAT			
GPIO21	SD_DATA2	DMIC**1**_CLK			
GPIO22	SD_DATA3				
GPIO23	CLK32K_INPUT	PWM8			
GPIO24	CLKOUT2				
GPIO25		DMIC**2**_DAT			
GPIO26		DMIC**2**_CLK			

All GPIO pins can wake up the internal MCU from standby mode and deep sleep mode. Any level change on the set GPIO will trigger the wake up procedure.

Function Name	Second Sets	Description
UART_TXD	UART2_TXD	UART TX data
UART_RXD	UART2_RXD	UART RX data
I2C_SCL		I2C clock
I2C_SDA		I2C data
IrDA		IrDA input
CaptureTime		Capture timer input
SPI_CSN		SPI chip enable
SPI_SCK	SPI2_SCK	SPI clock
SPI_MOSI	SPI2_MOSI	SPI master output slave input
SPI_MISO	SPI2_MISO	SPI master input slave output
CLKOUT		Analog clock output, (1/2/4/8/16) divided clock from 26 MHz crystal frequency or I2S DPLL (around 50 MHz)
PWM0~8		PWM waveform output
SD_CLK		SD card clock
SD_CMD		SD card command
SD_DATA0		SD card data0
SD_DATA1		SD card data1
SD_DATA2		SD card data2
SD_DATA3		SD card data3
JTAG_TCK		JTAG clock
JTAG_TMS		JTAG TMS
JTAG_TDI		JTAG TDI
JTAG_TDO		JTAG TDO
TX_EN		Indicator of Bluetooth transmitter is active
RX_EN		Indicator of Bluetooth receiver is active
PCM_SYNC		I2S or PCM synchronization or symbol signal
PCM_CLK		I2S or PCM bit clock signal
PCM_DIN		I2S or PCM data input signal
PCM_DOUT		I2S or PCM data output signal

CLK32K_INPUT		External 32 kHz XTAL input
CLKOUT2		Digital clock output, (1/2/4/8) divided clock from 26 MHz crystal frequency or I2S DPLL (around 50 MHz)
DMIC**1**_DAT	DMIC**2**_DAT	Digital microphone data input
DMIC**1**_CLK	DMIC**2**_CLK	Digital microphone clock output

4.10. Timer and Watch Dog Timer

There are two sets of timers. One set (fast) uses 1 MHz clock as the main clock, and another set (slow) uses divided 100 kHz clock as main clock. Each set has three 16-bit counters with 4-bit pre-divider.

The watch dog timer runs from the RC 100 kHz clock and has a maximum programmable period of up to 10.48 (2^16/100kHz * 16) seconds.

4.11. PWM output

There are nine PWM timers to provide six PWM output on GPIO. All the timers run with the same frequency, which can be either 26 MHz clock or low power clock.

The PWM timer has 16 bit resolution, with 1~16 pre scalar.

4.12. I2C and UART Interface

There are one I2C interface and two UART interfaces for debug or external MCU control of the BK3268.

The I2C clock rate can be from 12 to 3072 divided frequency from 26 MHz clock.

The UART clock rate can be from 3.2 kHz to 6.5 MHz.

4.13. SPI Interface

There are two sets of high speed full duplex SPI interface, which can be used as an interface for an external memory or LCD controller.

The SPI clock rate is from 50.8 kHz to 6.5 MHz when acts as master, and can be 6.5 MHz maximum as slave.

4.14. General Purpose SAR ADC

The general purpose SAR ADC has 10-bit resolution with a programmable sampling rate range from 5 kHz up to 50 kHz and is used to measure DC and low frequency voltages. The input voltage range for the ADC is from 0V to 3V. The general purpose ADC has eleven channels as table below.

Channel Number	Detected Voltage	Description
0	VCCBAT	Monitor battery voltage(0.65*VBAT)
1	GPIO2	GPIO2 voltage
2	GPIO19	GPIO19 voltage
3	VCC5USB	Monitor USB voltage(0.5*VUSB)
4	GPIO11	GPIO11 voltage
5	Temp-Sensor	Temp-Sensor Output voltage
6	GPIO13	GPIO13 voltage
7	GPIO14	GPIO14 voltage
8	GPIO25	GPIO25 voltage
9	GPIO26	GPIO26 voltage
10	GPIO15	GPIO15 voltage

4.15. SDIO Card Interface and USB interface

BK3266 includes a secure digital input output (SDIO) card interface. It supports either 1-bit mode, 2-bit mode or 4-bit mode. The initial clock rate is 203.125 kHz and can be up to 13 MHz.

The USB interface supports both host and device mode, with full speed.

4.16. IrDA interface

There is a hardware IrDA decoder interface to decode the signal. Also the interface has the capture timer capability to allow software decoding the input signal.

4.17. I2S interface

The I2S interface supports both master and slave mode, with sample rate from 7.35 kHz to 384 kHz.

There is an I2S DPLL dedicate for I2S and audio ADC/DAC. The I2S DPLL clock frequency is around 50 MHz that it could be 1024*FS for FS is 44.1 kHz or 44.8 kHz, or 8192*FS for FS is 8 kHz. The DPLL clock is a fractional PLL which is locked to 26 MHz crystal clock, and has less than 1 Hz tunable resolution.

4.18. QSPI Interface

The QSPI is designed for FLASH and RAM extension. The data IO are time shared by FLASH and RAM, while dedicate clock and select signal are separately used by FLASH and RAM. The QSPI can work up to 120 MHz, and FLASH clock and RAM clock can be set different.

4.19. eFUSE

The 32 byte eFUSE could be written through GPIO0 and GPIO1 together with 2.5 V applied to VCC2P5 at active mode, and only high 16 byte could be read out by GPIO. All the eFUSE content could be read by MCU without consideration of VCC2P5.

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Parameter	Description	MIN	TYP	MAX	Unit
VCCBAT	Battery regulator supply voltage	2.8		4.2	V
VCC5USB	USB power supply voltage	4.75		5.75	V
VCCBT	BT transceiver supply voltage	1.6		2.4	V
VCCAUD	Audio supply voltage	1.6		2.4	V
VCC3XTAL	Crystal supply voltage	2.8		3.8	V
P_{RX}	RX input power	-	10	-	dBm
T_{STR}	Storage temperature range	-40	-	150	℃

5.2. Recommended Operating Conditions

Parameter	Description	MIN	TYP	MAX	Unit
VCCBAT	Battery regulator supply voltage	2.8	3.6	4.2	V
VCC5USB	USB power supply voltage	4.75	5	5.75	V
VCCBT	BT transceiver supply voltage	1.6		2.4	V
VCCAUD	Audio supply voltage	1.6		2.4	V
VCC3XTAL	Crystal supply voltage	2.8		3.8	V
T_{OPR}	Operation temperature range	-20	-	80	℃

5.3. System LDO

Parameter	Description	MIN	TYP	MAX	Unit
VCCBAT	Battery input voltage	2.8		4.2	V
VCC3SYS	LDO output voltage	2.8	3.2	3.8	V
Load Current	Load current			200	mA

5.4. USB LDO

When USB is plug in, VCC3SYS will be generated from USB LDO.

Parameter	Description	MIN	TYP	MAX	Unit

VCC5USB	USB Input voltage	4.75	5	5.75	V
VCC3SYS	LDO output voltage		3.3		V
Load Current	Load current			200	mA

5.5. BATTERY CHARGE

Parameter	Description	MIN	TYP	MAX	Unit
VCC5USB	Charger input voltage	4.75	5	5.75	V
I_trickle	Charge Current at trickle mode as percent of fast charge mode		10		%
I_fast	Charge current at fast charge mode	40		220	mA
V_end(Need Calibrated)	VBAT voltage when Charge End		4.2		V

5.6. Analog LDO/BUCK

System can choose the analog BUCK or LDO as the power supply of RF and Audio part.

Parameter	Description	MIN	TYP	MAX	Unit
Analog LDO					
VDDANA	Analog LDO output voltage	1.6	1.8	2.4	V
Load Current	Load current			150	mA
Analog BUCK					
VDDANA	Analog BUCK output voltage	1.6	1.8	2.4	V
Load Current	Load current			150	mA
Switching frequency	BUCK modulation frequency	0.5	1	6	MHz

5.7. Digital LDO/BUCK

System can also choose the digital BUCK or LDO as the power supply for the Digital part.

Parameter	Description	MIN	TYP	MAX	Unit
Digital LDO					
VDDDIG	Digital LDO output voltage	1	1.2	1.35	V
Load Current	Load current			40	mA

Digital BUCK					
VDDDIG	Digital BUCK output voltage	1	1.2	1.35	V
Load Current	Load current			40	mA
Switching frequency	BUCK modulation frequency	0.5	1	6	MHz

5.8. Crystal and Reference Clock

Parameter	Description	MIN	TYP	MAX	Unit
Frequency	Crystal and Reference frequency	-	26	-	MHz
Tolerance	Crystal and Reference frequency tolerance	-10	-	+10	ppm
XI Pin	Input voltage range for reference clock input	-0.3		3.6	V

5.9. Typical Power Consumption

State	Description	MIN	TYP	MAX	Unit
Shut Down	Software sets device into shut down mode, wake up from GPIO15		0.4	0.8	uA
Standby	Software sets device into standby mode, wake up from GPIO and RTC timer		4	6	uA
Idle-Sniff	Idle state at Sniff mode		300		uA
Active (A2DP)	2DH5		9		mA
Active (HFP)	HV1		9.5		mA

5.10. RF Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
Operate Frequency	2402~2480	2402		2480	MHz
RXSENS-1 Mbps	BER=0.001		-91		dBm
RXSENS-2 Mbps	BER=0.0001		-93		dBm
RXSENS-3 Mbps	BER=0.0001		-85		dBm
Maximum received signal	BER=0.001	0			dBm

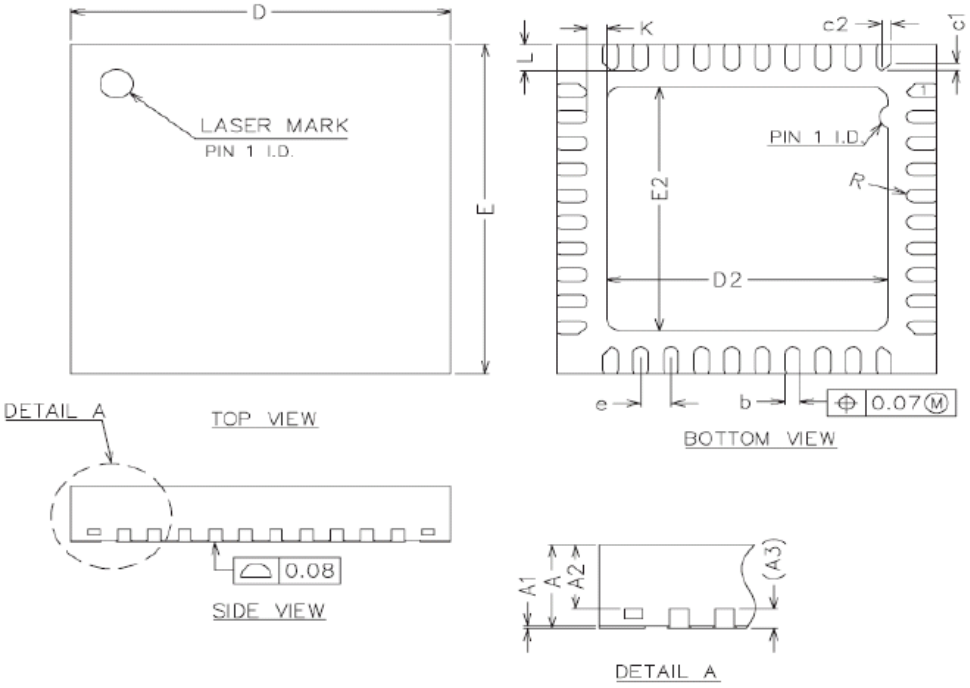
Maximum RF transmit power			8		dBm
RF Power Control Range		30			dB

5.11. Audio Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
DAC Diff. Output Amplitude	With 600ohm loading			1.1	Vrms
	With 32ohm loading		-	-	Vrms
	With 16ohm loading			0.9	Vrms
DAC Diff. Output THD	With 1.1Vrms@600ohm loading		84		dB
	With 0.8Vrms@16ohm loading		80		dB
DAC output SNR	1 kHz sine wave		104		dB
DAC Sample Rate		8		48	kHz
Audio Output Gain		-34		6	dB
Audio Output Gain Step			1		dB
Audio Output Channel Separation	Full Differential		90		dB
Common mode	VCOM		1.5		V
Microphone Gain		0		42	dB
Microphone Gain Step			2		dB
Microphone Reference	MICREF		2.5		V
Audio Input Channel Separation			100		dB
ADC Sample Rate		8		48	kHz
ADC SNR	1 kHz sine wave		96		dB

6. Package Information

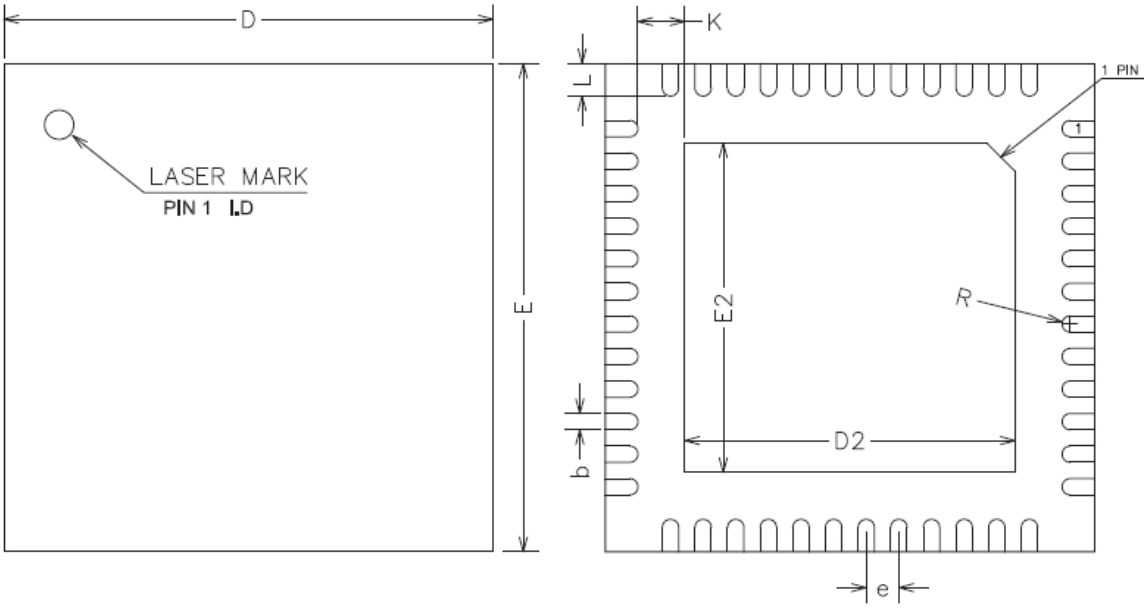
6.1. QFN 5x5 40-Pin

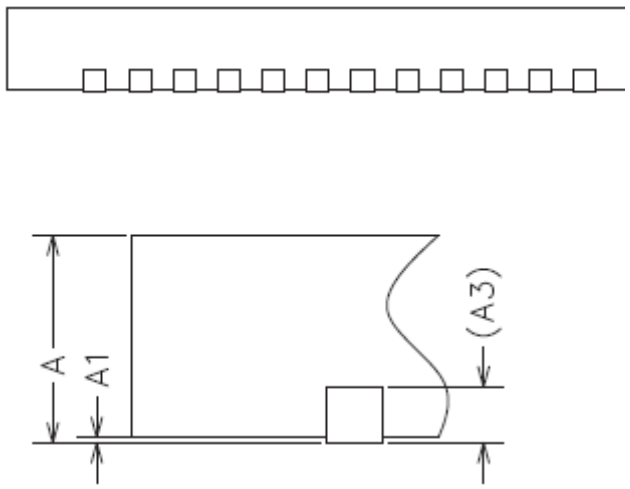


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.50	0.65	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
C1	–	0.12	–
C2	–	0.12	–

6.2. QFN 6x6 48-Pin

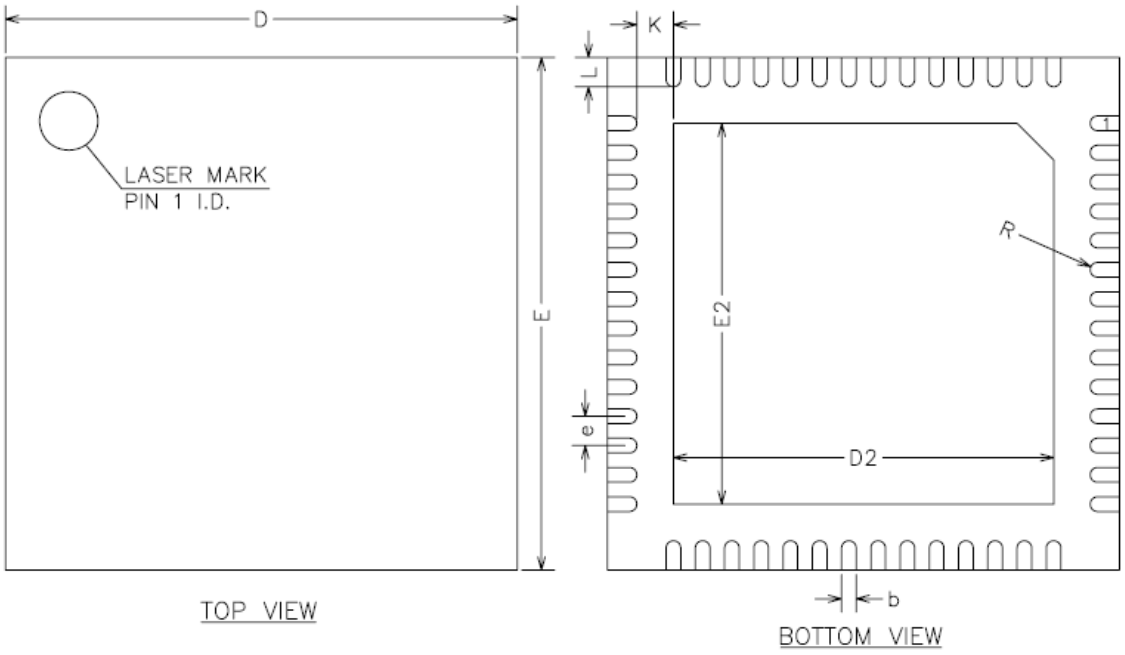




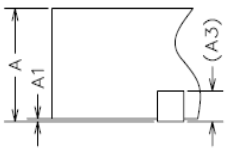
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

6.3. QFN 7x7 56-Pin



SIDE VIEW



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.05	5.20	5.35
E2	5.05	5.20	5.35
e	0.30	0.40	0.50
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

7. Ordering Information

Part number	Package	Packing	MOQ (ea)
BK3268QN40A	QFN 5mmx5mm 40-Pin	Tape Reel	3 k
BK3268QN40B	QFN 5mmx5mm 40-Pin	Tape Reel	3 k
BK3268QN48	QFN 6mmx6mm 48-Pin	Tape Reel	3 k
BK3268QN56	QFN 7mmx7mm 56-Pin	Tape Reel	3 k

Remark:

MOQ: Minimum Order Quantity