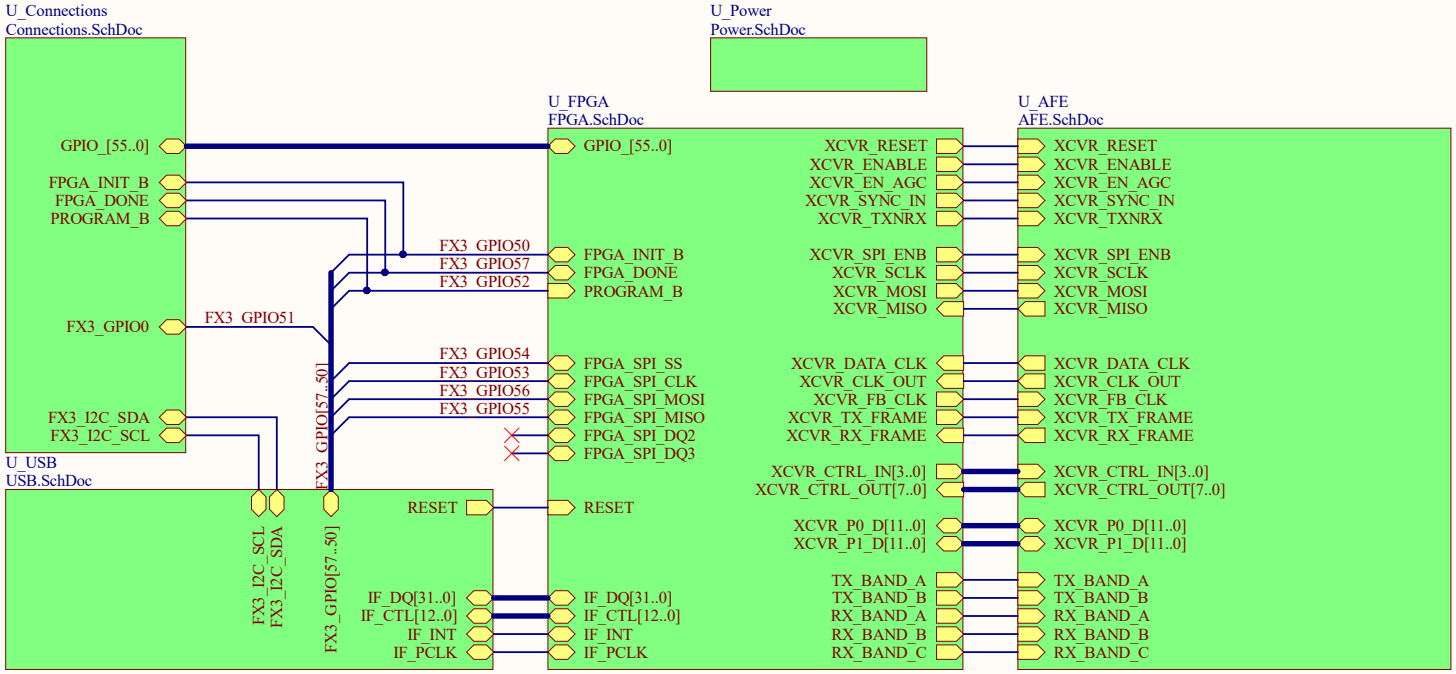
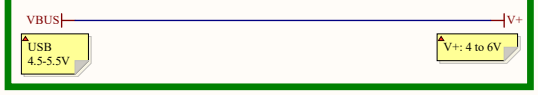
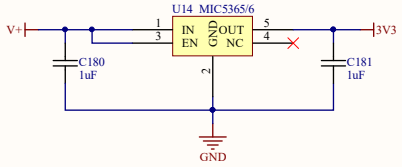


Title	**FreeSRP**		
Size	Number		Revision
A4	**1**		**2**
Date:	4/13/2017	Sheet 1 of 7	
File:	FreeSRP.SchDoc	Drawn By: Lukas Lao Beyer	

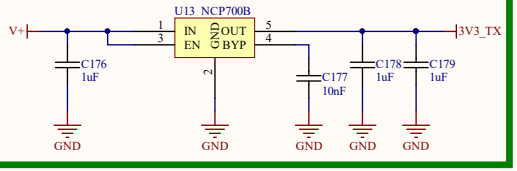
BUS/EXTERNAL POWER SELECTION



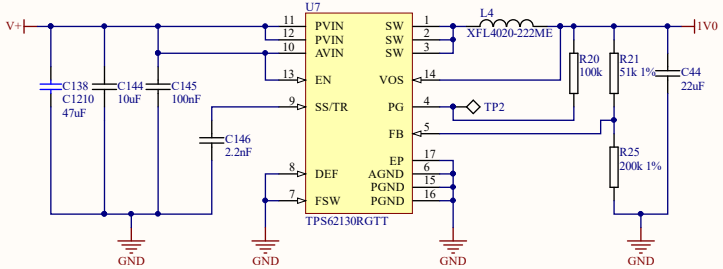
3V3: 3.30V, 0.15A



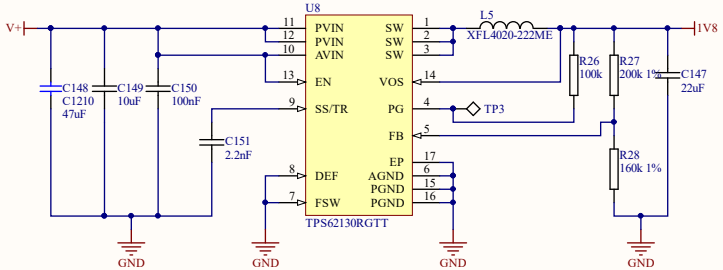
3V3_TX: 3.30V, 0.2A



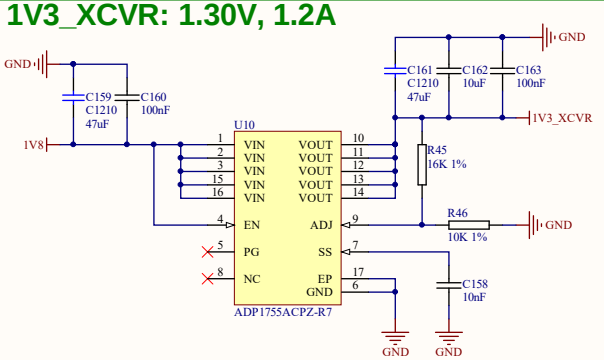
1V0: 1.00V, 3A



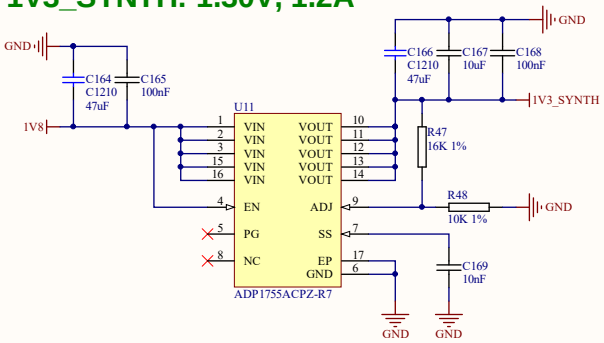
1V8: 1.80V, 3A



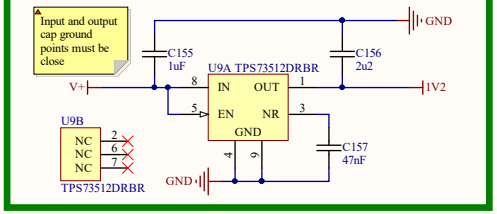
1V3_XCVR: 1.30V, 1.2A



1V3_SYNTH: 1.30V, 1.2A

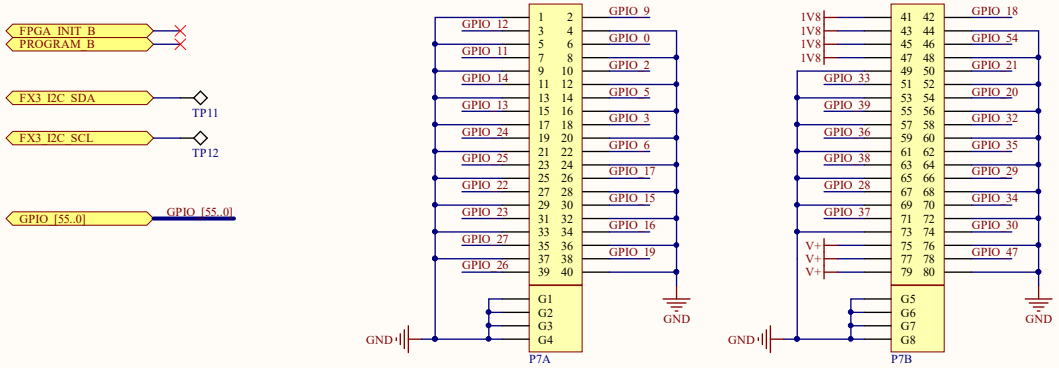


1V2: 1.20V, 0.5A

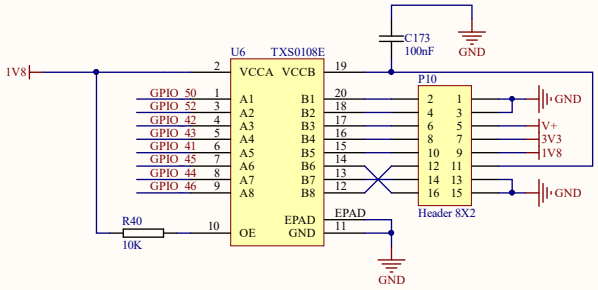


Title: **Power**		
Size: A3	Number: **2**	Revision: **2**
Date: 4/13/2017		Sheet 2 of 7
File: Power.SchDoc		Drawn By: Lukas Lao Beyer

EXPANSION HEADERS

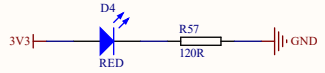


LEVEL SHIFTED GPIO

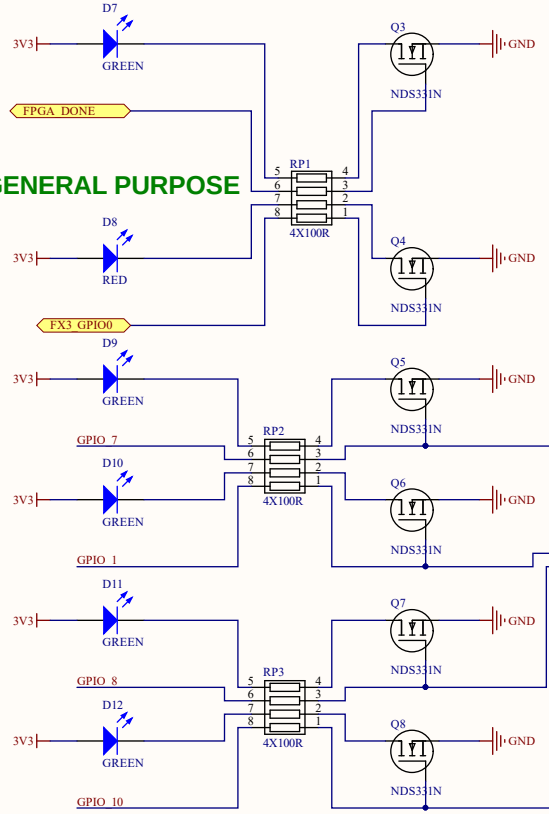


LED INDICATORS

POWER INDICATORS



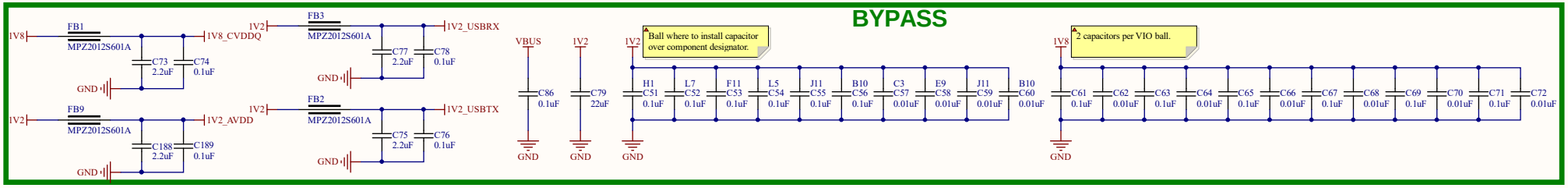
FPGA DONE



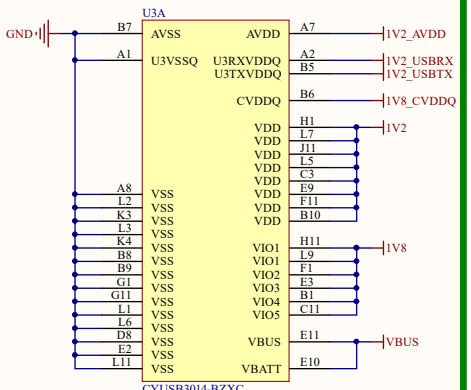
GENERAL PURPOSE

Title	**Expansion Connectors and Status LEDs**	
Size: A3	Number: **3**	Revision: **2**
Date: 4/13/2017		Sheet 3 of 7
File: Connections.SchDoc		Drawn By: Lukas Lao Beyer

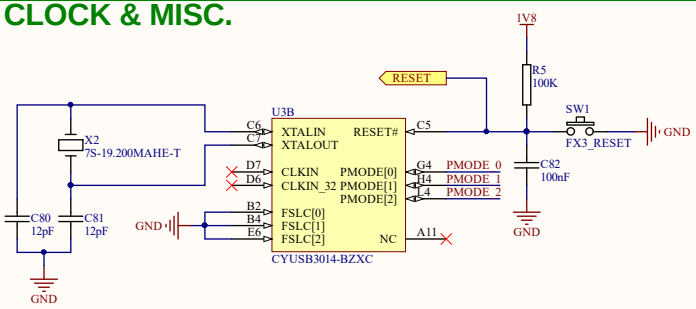
BYPASS



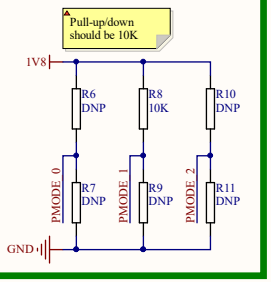
POWER



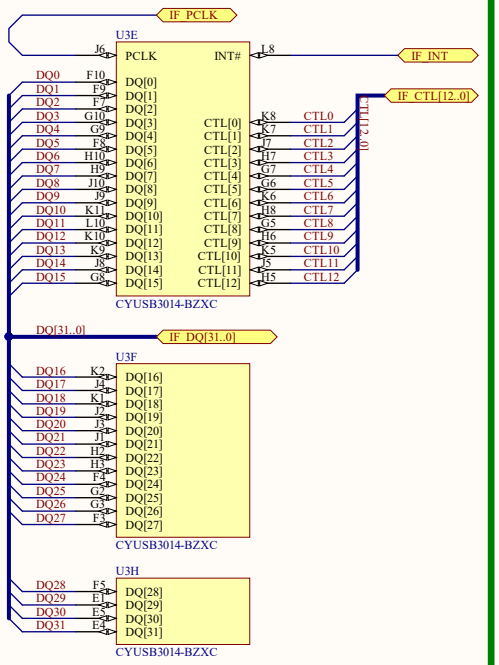
CLOCK & MISC.



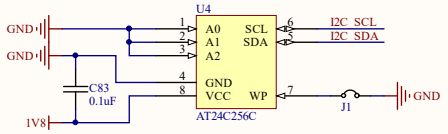
BOOT MODE SEL.



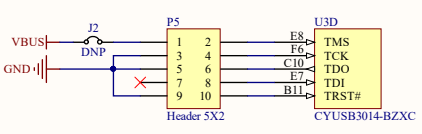
GPIF II FPGA INTERFACE



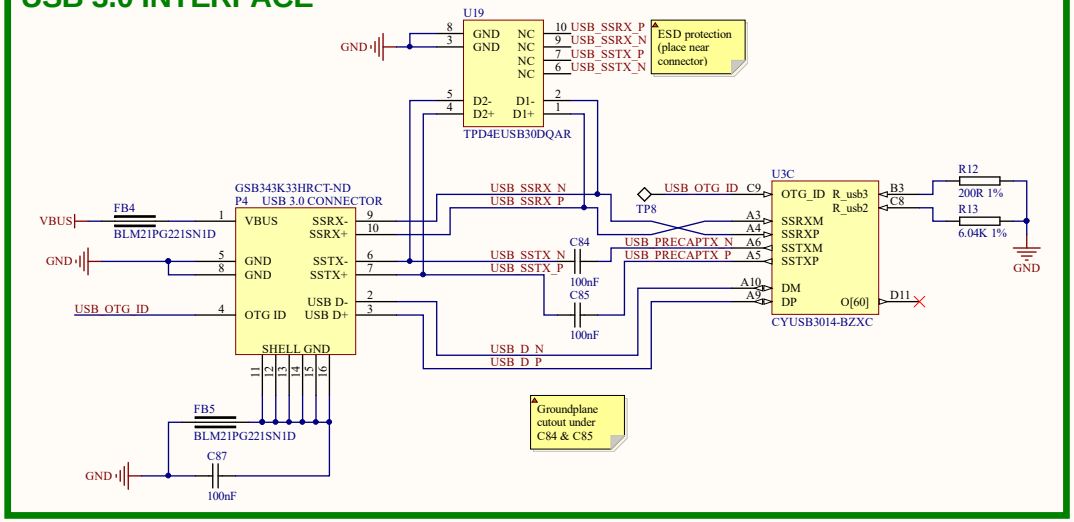
FX3 BOOT FLASH MEMORY



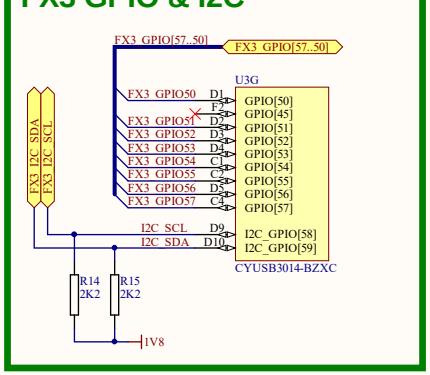
JTAG



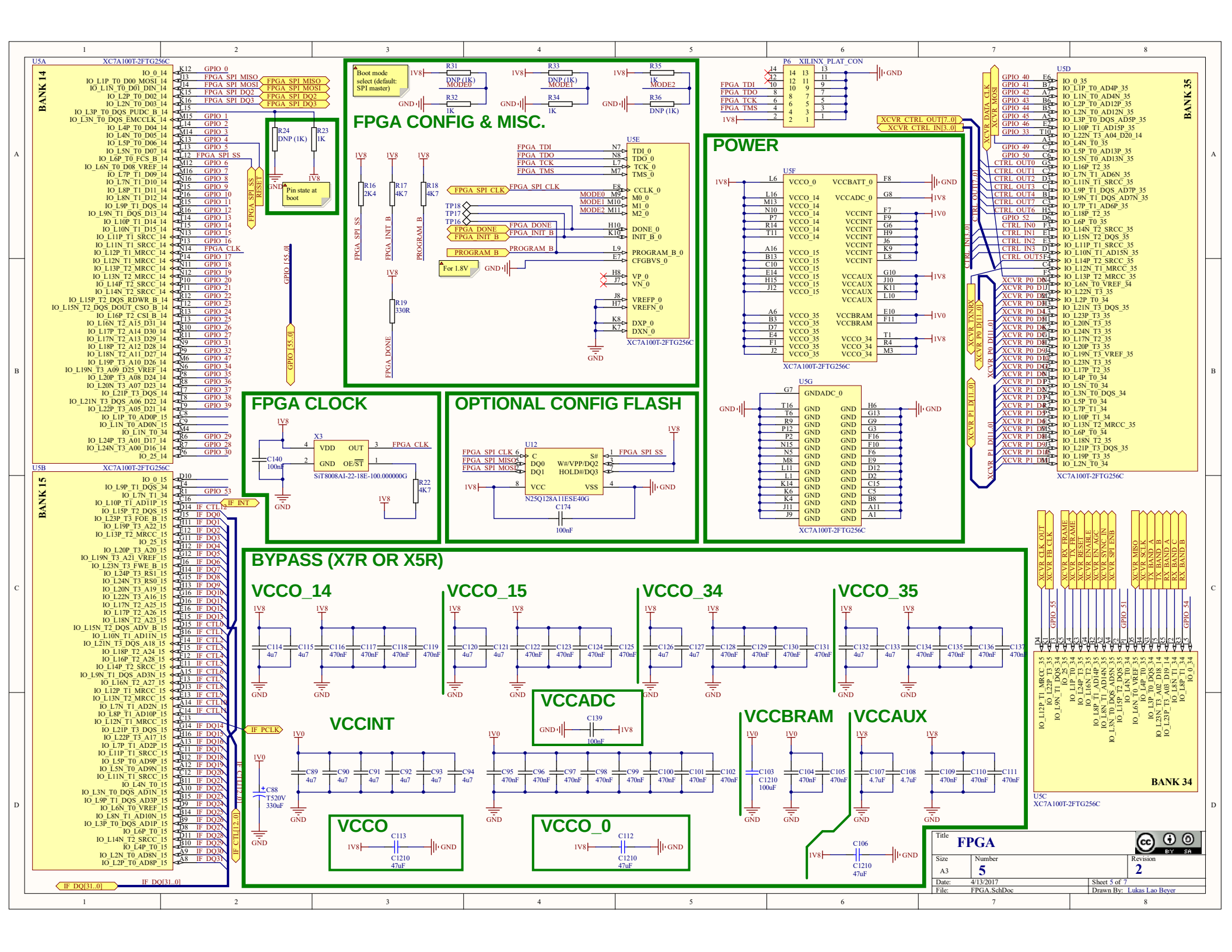
USB 3.0 INTERFACE

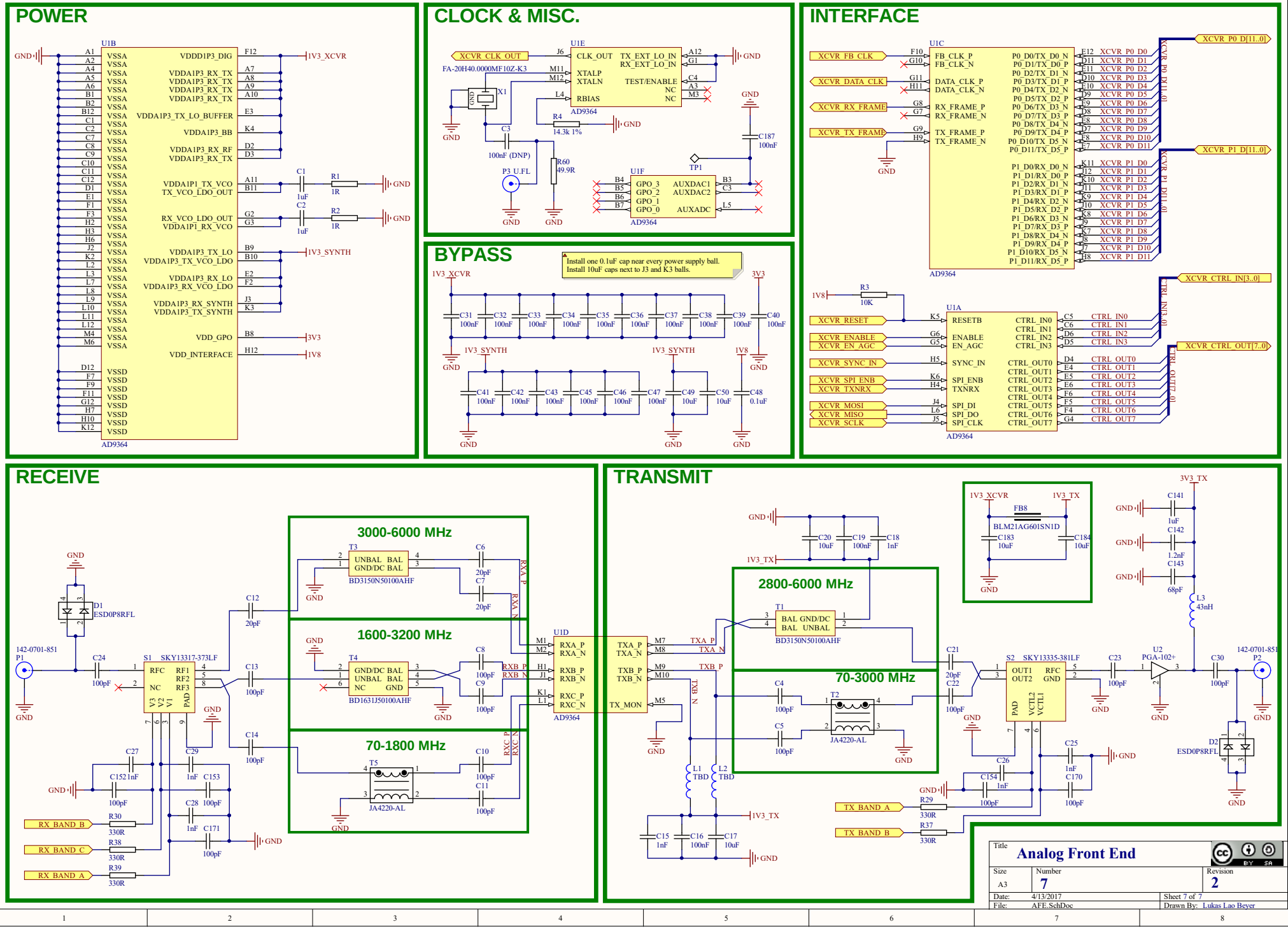


FX3 GPIO & I2C



Title: **USB Interface**		
Size: A3	Number: **4**	Revision: **2**
Date: 4/13/2017	Sheet 4 of 7	
File: USB.SchDoc	Drawn By: Lukas Lao Beyer	


FPGA CONFIG & MISC.
POWER
FPGA CLOCK
OPTIONAL CONFIG FLASH
BYPASS (X7R OR X5R)
VCCO_14
VCCO_15
VCCO_34
VCCO_35
VCCINT
VCCADC
VCCBRAM
VCCAUX
VCCO
VCCO_0
BANK 14
BANK 15
BANK 34
BANK 35
U5A XC7A100T-2FTG256C
U5B XC7A100T-2FTG256C
U5C XC7A100T-2FTG256C
U5D XC7A100T-2FTG256C
U5E XC7A100T-2FTG256C
U5F XC7A100T-2FTG256C
U5G XC7A100T-2FTG256C
P6 XILINX_PLAT_CON
X3 SiT8008AI-22-18E-100.000000G
U12 N25Q128A11ESE40G
Boot mode select (default: SPI master)
Pin state at boot
For 1.8V
Title FPGA
Size A3
Number 5
Revision 2
Date: 4/13/2017
File: FPGA.SchDoc
Sheet 5 of 7
Drawn By: Lukas Lao Beyer


POWER
U1B
AD9364
1V3_XCVR
1V3_SYNTH
3V3
1V8
GND
CLOCK & MISC.
U1E
XCVR_CLK_OUT
FA-20H40.0000MF10Z-K3
X1
14.3k 1%
100nF (DNP)
P3_U.FL
TP1
U1F
AUXDAC1
AUXDAC2
AUXADC
BYPASS
Install one 0.1uF cap near every power supply ball.
Install 10uF caps next to J3 and K3 balls.
INTERFACE
U1C
XCVR_FB_CLK
XCVR_DATA_CLK
XCVR_RX_FRAME
XCVR_TX_FRAME
XCVR_P0_D[11..0]
XCVR_P1_D[11..0]
U1A
XCVR_RESET
XCVR_ENABLE
XCVR_EN_AGC
XCVR_SYNC_IN
XCVR_SPI_ENB
XCVR_TXNRX
XCVR_MOSI
XCVR_MISO
XCVR_SCLK
XCVR_CTRL_IN[3..0]
XCVR_CTRL_OUT[7..0]
RECEIVE
3000-6000 MHz
1600-3200 MHz
70-1800 MHz
BD3150N50100AHF
BD1631J50100AHF
JA4220-AL
SKY13317-373LF
ESD0P8RFL
RX_BAND_A
RX_BAND_B
RX_BAND_C
TRANSMIT
2800-6000 MHz
70-3000 MHz
BD3150N50100AHF
JA4220-AL
SKY13335-381LF
PGA-102+
BLM21AG601SN1D
TX_BAND_A
TX_BAND_B
Title
Analog Front End
Size
A3
Number
7
Revision
2
Date:
4/13/2017
Sheet 7 of 7
File:
AFE.SchDoc
Drawn By:
Lukas Lao Beyer